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MODULAR DIGITAL RADIO FREQUENCY (RF) RECEIVER SYSTEM (MODRFS) PROGRAM

System Architecture Study

Dr. Lawrence Scanlan

Raytheon Company
Electronic Systems
P.O. Box 902
El Segundo, CA 90245-0902

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AIR FORCE RESEARCH LABORATORY
AIR FORCE MATERIEL COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7318

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LT JASON A SHTRAX, USAF
Contract Monitor
Reference Sensors & Receiver Applications Branch
RF Sensor Technology Division

DR STEPHEN HARY
Supervisor
Reference Sensors & Receiver Applications Branch
RF Sensor Technology Division

WILLIAM E MOORE, CHIEF
RF Sensor Technology Division
Sensors Directorate

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The objective of the MODRFS program architecture study was to further refine the modular RF system concept by examining the targeted radar and Electronic Warfare (EW) application requirements and defining and RF electronics module set and RF building blocks that implement the concept consistent with these application requirements. The requirements and architecture for a multifunction radar receiver were specifically defined along with detailed building block specifications. In addition, the applicability of the RF building blocs to air-to-ground reconnaissance and Communication, Navigation, and Identification (CNI) applications are assessed.

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1. INTRODUCTION

1.1 BACKGROUND AND STUDY OVERVIEW

Currently planned and contemplated airborne weapon systems require expanded RF sensor capabilities while both legacy avionics upgrades and new developments have a definite need to reduce acquisition and support cost. At the same time, limited development resources and a desire for shortened development cycles invite approaches that maximize design reuse and are suitable for a broad set of applications. A modular RF system concept directly addresses the challenging and conflicting demands presented by this situation.

The need for expanded capabilities and enhanced performance is addressed by leveraging recent and anticipated technology advances. In addition, the system architecture encapsulates various functional elements by imposing isolation layers at key physical/functional boundaries, localizing the effect of implementation details. This allows the system to gracefully incorporate technology advances without design changes in one area rippling throughout the entire system and triggering large verification/validation efforts. The encapsulation layers also expand retrofit options by allowing mixed old and new configurations.

Hardware reuse is promoted in two ways. The architecture is segmented into functional subsystems made up of plug in modules. Different system configurations can be constructed for various applications by varying the type and number of modules used. The modules themselves are made up of functional building blocks that can be reused across module types.

The functional encapsulation concept also greatly enhances software portability from one application to another. The encapsulation layer at the sensor hardware/software boundary is part of a software architecture designed to very efficiently handle multimode scheduling in a shared resource system. This architecture provides a uniform framework for handling multiple sensors and modes including Built In Test and System Calibration. It also provides the sockets for application portable mode and sensor software.

The modular RF sensor system, made up of apertures, RF electronics, and processing, is shown in Figure 1.1-1. The apertures are defined by the platform and mission specifics, while the RF electronics, processing hardware, and sensor software can be tailored to achieve specific sensor capabilities and performance. The RF signal distribution and aperture control functions at the aperture/RF electronics boundary are relatively straightforward functions adapted to the specific application. The interconnection network at the RF electronics/processing boundary distributes control and sensor data among the modular processing nodes and the nearest layer of the RF electronics. It provides a flexible interconnection fabric for the multi-node processor, supporting a scalable mix of general purpose data processing and special purpose signal processing modules. In addition it is a key element of the isolation layer between the RF electronics and sensor software. The digital preprocessor could include special signal processing functions such as pulse compression, beam forming, or waveform parameter extraction depending on the application.

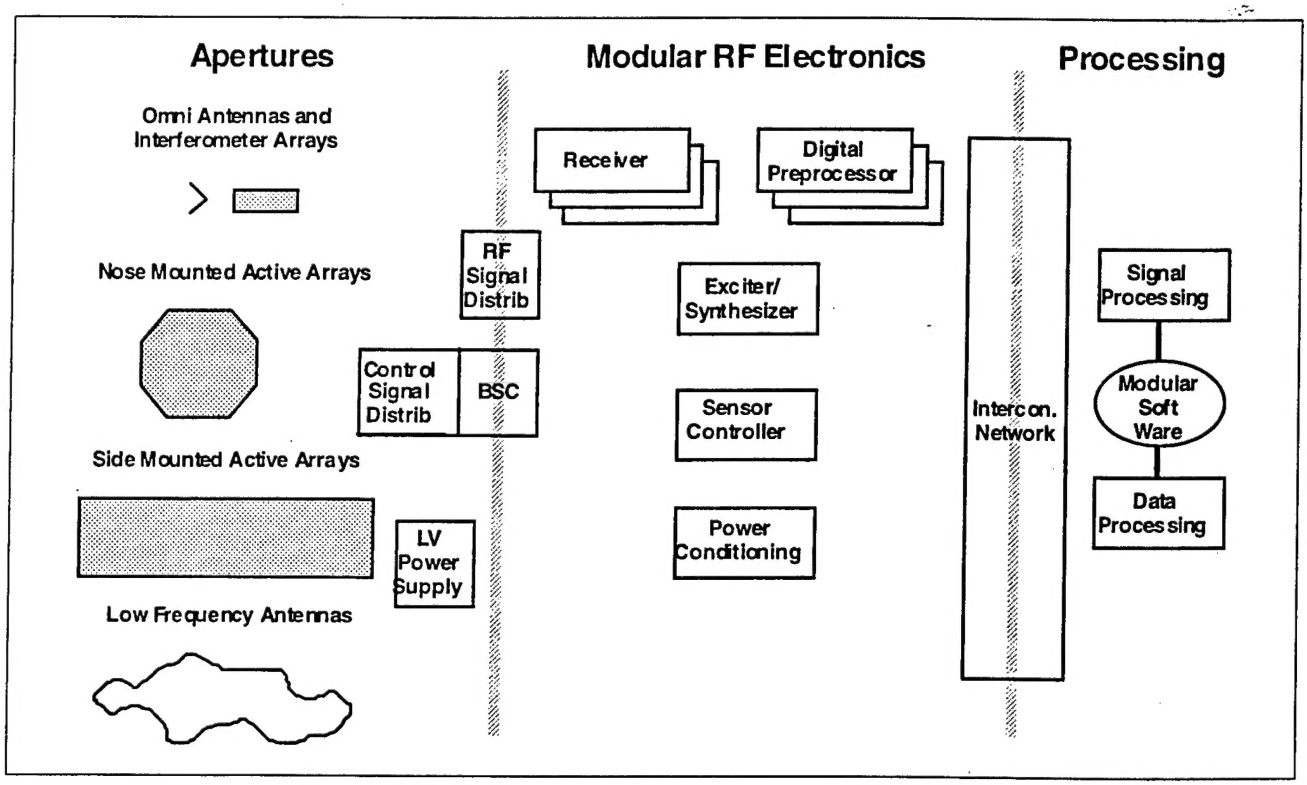

Figure 1.1-1. Modular RF Sensor System Architecture

1.2 STUDY OBJECTIVE AND APPROACH

The objective of the MODRFS program architecture study was to further refine the modular RF system concept by examining the targeted radar and Electronic Warfare (EW) application requirements and defining an RF electronics module set and RF building blocks that implement the concept consistent with these application requirements. The requirements and architecture for a multifunction radar receiver were specifically defined along with detailed building block specifications. In addition, the applicability of the RF building blocks to air-to-ground reconnaissance and Communication, Navigation and Identification (CNI) applications are assessed. The results of this study are documented in the following sections.

2. TOP LEVEL REQUIREMENTS DEFINITION

Since the primary objective of the MODRFS program is to define and develop receiver building blocks that can support a wide variety of applications, the requirements effort focused on determining the major functions performed by the systems described above. These functions are shown in Figure 2-1.

As can be seen from the figure, there are a large variety of functions that could be performed by a common set of receiver building blocks. Due to the large number of functions, the fact that specific requirements for each function are typically different depending on the platform, and the various classification levels of these requirements, an attempt to define specific requirements for these functions was not made. Instead, a set of key requirements was defined at a receiver subsystem level. These receiver subsystem requirements, which are described in Section 5 herein, were developed with the intention of balancing criteria such as cost, weight and volume while still performing the majority of functions shown in Figure 2-1 at a level of performance that would satisfy most applications.

In addition to the functional requirements described above, an attempt was made to define a set of key "non-functional" requirements. These are requirements that are not traceable to a specific system function but are still critical for meeting overall system performance. Key non-functional requirements identified for further study were module form factor, cooling method, environment, control interface definition, and the ability to backfit into legacy systems. These requirements are addressed further in the Section 6 of this report.

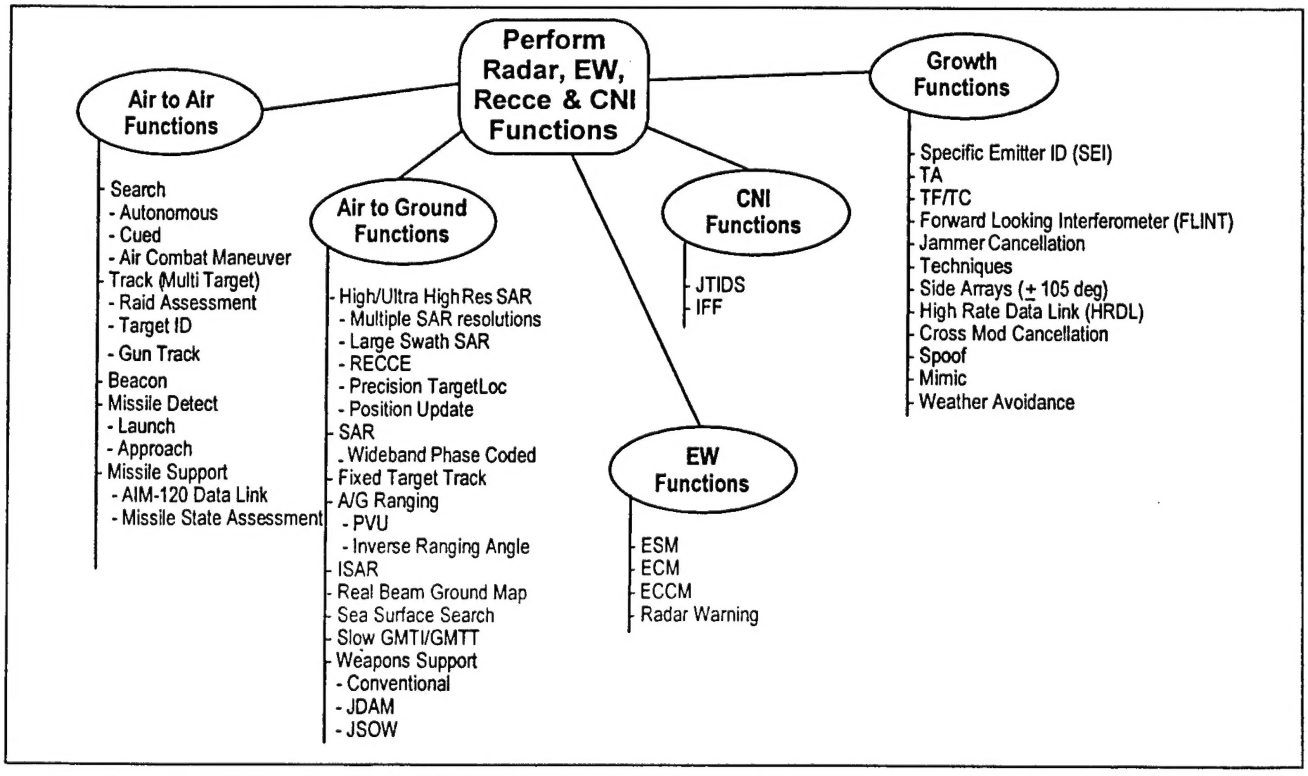

Figure 2-1. Typical Radar, EW and CNI Functions.

3. MODULAR BUILDING BLOCK CONCEPT

Five specific applications, Multifunction Radar, A/G Reconnaissance Radar, A/A and A/G Surveillance Radar and an ESM Receiver, were considered for the implementation of the modular RF system concept. The RF electronics for these applications can be implemented by the following common module set:

Narrowband Receiver Front End – A high dynamic range receiver front end suitable for A/A and look down A/A radar applications. The tunable range covers X-Band and extends into C and Ku bands. The instantaneous bandwidth is 200 MHz. Note: It is still under study whether this receiver bandwidth should be extended to 400 to 600 MHz, or if another class of receiver should be added to the module set.

Low Band Receiver Front End – A high dynamic range receiver front end suitable for long range A/A surveillance applications. Tunable range covers L and S bands. The instantaneous bandwidth is 60 MHz. (Note that similar to this Low Band Receiver Front End approach, a High Band Receiver Front End could be added to satisfy requirements for a Ku band system).

Narrowband Preprocessor – Accepts ADC input from a Narrowband or Low Band Receiver module and performs matched filtering, IQ formation, data distribution, receiver/exciter control and AGC processing functions. This module could be expanded to include a programmable pulse compression function.

Wideband Downconverter – Provides low noise amplification and block converts the ESM Receiver RF band to the acquisition receiver input IF.

Acquisition Receiver – Channelizes a wideband input into a bank of narrowband filters. Detects activity in each channel and extracts pulse parameters.

X-Band Exciter – Synthesizes X-band radar high fidelity transmit and receiver LO reference waveforms and clocks. Note, this function would require more than one module at the current state-of-the-art.

Low Band Exciter – Synthesizes low frequency radar high fidelity transmit and receiver LO reference waveforms and clocks. This function would require more than one module at the current state-of-the-art. (Note that similar to this Low Band Exciter approach, a High Band Exciter could be added to satisfy requirements for a Ku band system).

Wideband Synthesizer – Synthesizes ESM receiver downconversion LO references and clocks. Note, this function would require more than one module at the current state-of-the-art.

Wideband Preprocessor – Performs cross channel processing of channelizer outputs. Extracts detected emitter waveform parameters and creates Pulse Descriptor Words.

Sensor Controller – Expands abstract API inputs into hardware micro commands. Supervises subsystem operation and self test.

RF Power Supply – Provides low ripple, low voltage power forms to the RF electronics.

The modules themselves are designed around reusable function elements called RF building blocks. The building blocks come in three forms:

Physical Building Blocks – A collection of circuit elements assembled together to perform a complex function. The X-Band Downconverter is an example of this type. It is made up of MMICs, filters, isolators, linear regulators, and control circuits packaged in a sealed microwave package.

Functional Building Blocks – A collection of circuit elements connected together to perform a complex function. Instead of a packaged part this building block is represented by a reference design and layout for a mix of off-the-shelf and custom prepackaged parts. The embedded controller is an example of this type. It is made up of a commercial microprocessor, memory and glue logic circuits.

Virtual Building Blocks – An HDL, macro, or schematic level circuit description that can be embedded as IP in a custom, semi-custom, or programmable IC. The RF control interface is an example of this type

A set of RF building blocks that could be used to implement the common module set is listed below. The module and building block mapping to applications are shown in Table 3-1. The building blocks were selected for their reuse potential or for their generality and functional complexity.

Wideband ADC – Samples the receiver IF signal and encodes it into a multi-bit digital word. Converts an IF bandwidth of 500 to 1000 MHz.

Narrowband ADC – Pulse code modulates the receiver IF signal using a Δ-Σ modulator. Converts an IF bandwidth of 60 to 180 MHz

RF Preselect Filter – Provides RF selectivity to protect the receiver against friendly or intentional Radio Frequency Interference (RFI).

X-Band Downconverter – Downconverts an X-band input to the receiver IF. Establishes the receiver noise figure and provides variable gain amplification.

Wideband Downconverter – Downconverts a 2-18 GHz input to the receiver IF. Establishes the receiver noise.

Digital Video Processor – Extracts the complex modulation envelope from a digital IF signal and performs matched filtering. Can accept single bit or multi-bit pulse coded inputs.

Digital Channelizer – Filters a wideband digital IF signal into 10 to 20 subbands and provides an activity indicator (i.e. threshold detector) and digital memory for the subband filter outputs.

Parameter Encoder – Extracts waveform parameters (e.g. time of arrival, pulsewidth, frequency, phase, etc.).from a digital IF signal.

Embedded Controller – Expands the abstract control interface into receiver subsystem and exciter subsystem microcommands and supervises receiver and exciter operation. Controls receiver front end gain. Used anywhere a sophisticated control function is required.

Wideband DDS – Digitally synthesizes a wide range of phase coded and frequency coded waveforms with bandwidths up to 600 to 1000 MHz.

Narrowband DDS – Digitally synthesizes a single frequency with specialized modulations.

Stable Oscillator– Low noise frequency source.

High Dynamic Range Upconverter – Converts intermediate frequencies from 1 to 3 GHz to X-band and provides power amplification.

Data/Control Network Interface –Fibre Channel Network Interface Controller. Used for high bandwidth data transport and low latency control functions.

RF Control Interface – Provides control interface to analog/RF modules.

Programmable Timing Generator– Provides programmable, precisely timed, low jitter gates and sync signals for radar or EW synchronization.

TABLE 3-1. MODULAR RF SYSTEM BUILDING BLOCKS AND APPLICATIONS

		Narrow Band Rcvr	Low Band Rcvr	Wide Band Dwn Cnvtr	Acq Rcvr	X-Band Exciter	Low Band Exctr	Wide Band Synth	Sensor Control	Narrow Band Preproc	Wide Band Pre-proc	RF Power Supply
APPLICATIONS	Multifunction Radar	✓				✓			✓	✓		✓
	A/G Surveillance Radar	✓				✓			✓	✓		✓
	A/A Surveillance Radar		✓				✓		✓	✓		✓
	Reconnaissance Radar	✓				✓			✓	✓		✓
	ESM Receiver	✓		✓	✓			✓	✓	✓	✓	✓
BUILDING BLOCKS	Wide Band ADC				✓							
	Narrow Band ADC	✓	✓									
	RF Preselection Filter	✓										
	X-Band Down Converter	✓										
	Wide Band Down Converter			✓								
	Digital Video Processor									✓		
	Digital Channelizer				✓							
	Parameter Encoder				✓							
	Embedded Controller				✓				✓	✓		
	Wide Band DDS					✓	✓					
	Narrow Band DDS					✓						
	Stable Oscillator					✓	✓					
	High Dynamic Range Up Conv.					✓	✓					
	Data/Control Netwrk Interface				✓				✓	✓	✓	
	RF Control Interface	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓
	Programmable Timing Gen.					✓	✓	✓			✓	

4. MULTI-ROLE FIGHTER SENSOR SYSTEM ARCHITECTURE

Figure 4-1 illustrates the modular building block approach applied to the Radar/ESM sensor system for a multirole fighter application. The figure shows the common modules configured into a narrowband subsystem and a wideband subsystem connected to a forward looking multifunction active array and wideband interferometer arrays in the four quadrants of the aircraft. This application was chosen because it has many elements in common with other applications and, as it is configured in Figure 4-1, introduces tightly integrated radar and ESM functions along with resource sharing of oversubscribed assets. This has implications for the system architecture, the software architecture, and the RF electronics.

The software architecture is modular and incorporates encapsulation layers to promote portability of application mode software. The application mode software is arguably the software with the longest potential life and, in actuality, is the least reused across current systems. The implementation includes two isolation layers surrounding the modes. The top isolation layer, between the mission software and the modes, supports mode reuse across platforms with different mission software. We have observed that this interface survives across many airborne and sea-based systems. Under this isolation layer, the plug-in modes are scheduled at a functional level. Under the modes, but above the MODRFS hardware, the bottom isolation layer provides a stable application programming interface between the MODRFS hardware and the modes. This supports stable mode software both across system applications and during the long life of any given system application.

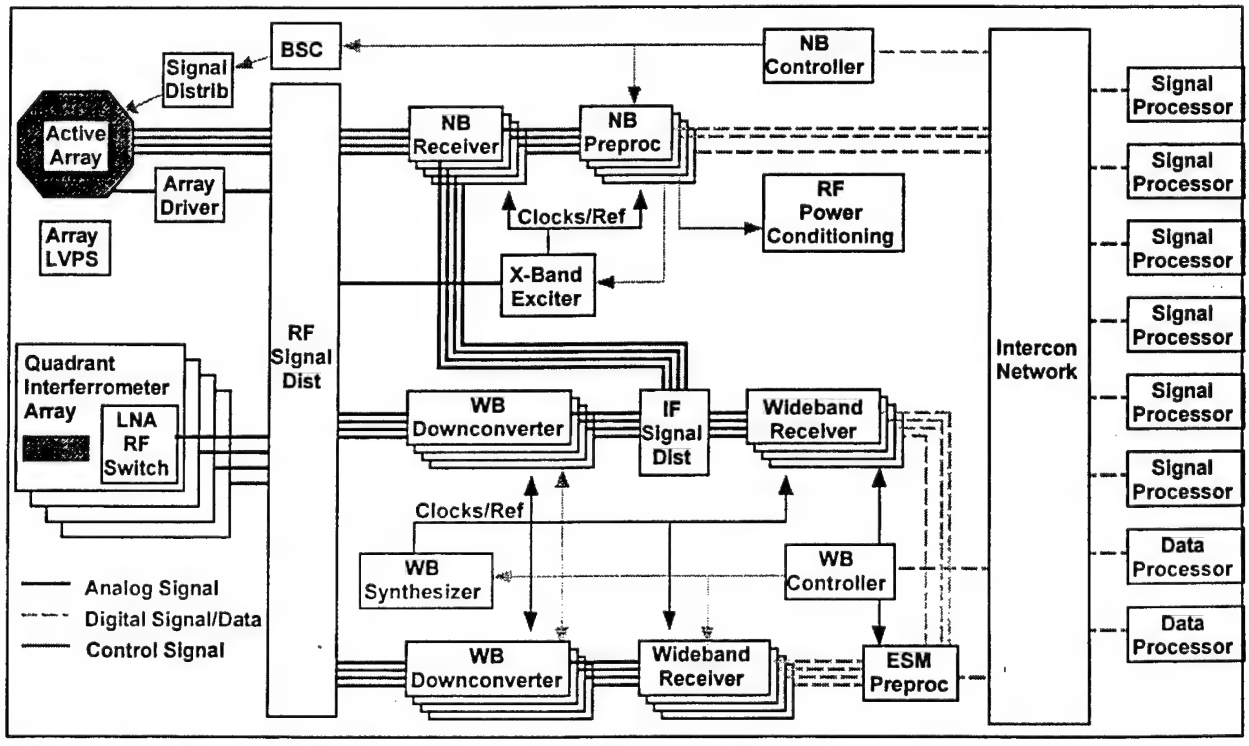

Figure 4-1. Multirole Fighter Radar/ESM Modular Sensor System

5. NARROWBAND RECEIVER SUBSYSTEM DEFINITION

As shown in Figure 4-1, the Narrowband Receiver module and the Narrowband Preprocessor module together form a narrowband receiver subsystem. A summary of the receiver subsystem requirements is shown in Table 5-1.

The building block architecture for these two modules is illustrated in Figure 5-1. The receiver is an IF sampling heterodyne receiver with the extra functions required to be consistent with the system architecture and implement the encapsulation layers. The physical partitioning shown in the figure is the result of a trade study described in Section 6.3, herein.

5.1 BUILDING BLOCKS DEFINITION

The following RF building blocks are used to construct the receiver subsystem: RF Preselect Filter, X Band Downconverter, Narrowband ADC, Digital Video Processor, Data/Control Network Interface, Embedded Controller, and RF Control Interface. The Data/Control Network Interface and RF Control Interface are described in Section 6.1; the remaining building blocks are described in the following sections.

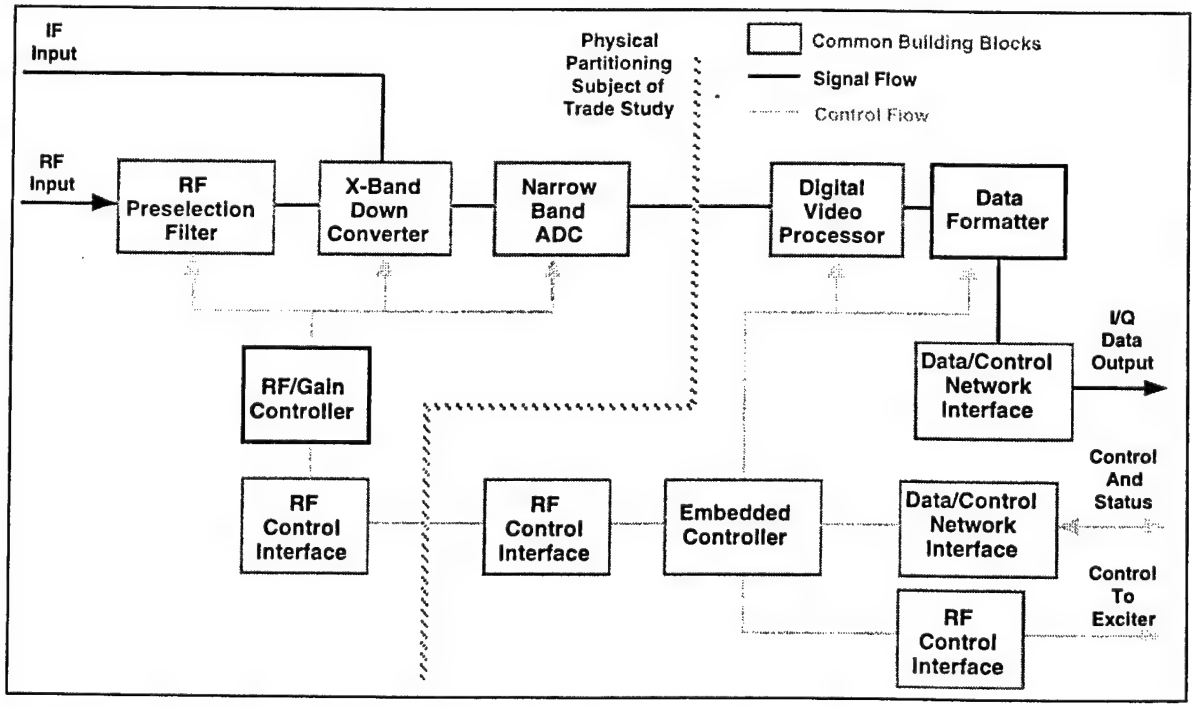

Figure 5-1. Narrowband Receiver Subsystem Functional Block Diagram

TABLE 5-1. NARROWBAND RECEIVER SUBSYSTEM REQUIREMENTS

RF Band	6 – 14 GHz
Programmable Video Bandwidth	0.5 to 60 MHz (0.5 to 180 MHz Growth)
Dynamic Range	77- 85 dB
SFDR	112 dB
Channel Match	60 dB
Channel Isolation	60 dB
RF Selectivity	Yes (approx 600 MHz bands)
Auxiliary IF Input	Yes
Automatic Gain Control	Yes

5.1.1 RF Preselect Filter

The RF preselect filter divides a wide band RF frequency input (on the order of 6-14 GHz) into manageable sub-bands as shown in Figure 5.1.1-1. The preselect filter is compact in size (2.4x1.3x0.5 inches), has fast switching speed (< 1.0 μs), low insertion loss (< 5.5 dB), high intercept point (> 45 dBm) and good input power handling (> 1 W). The filtering is applicable to active array applications, where the array establishes the system noise figure and has sufficient amplification to overcome the insertion loss of the filters.

5.1.1.1 RF Preselect Filter Performance. The RF preselect filter contains 14 switch-selectable bandpass filters to restrict the input frequency band to the region of interest and to exclude out of band interference. Eleven channels are X-Band filters as defined in Table 5.1.1.1-1. The remaining channels include a through line path, a 9 to 10 GHz analog power monitor, and a 50 ohm matched termination. The path selection is internally decoded from four input bits according to Table 5.1.1.1-2.

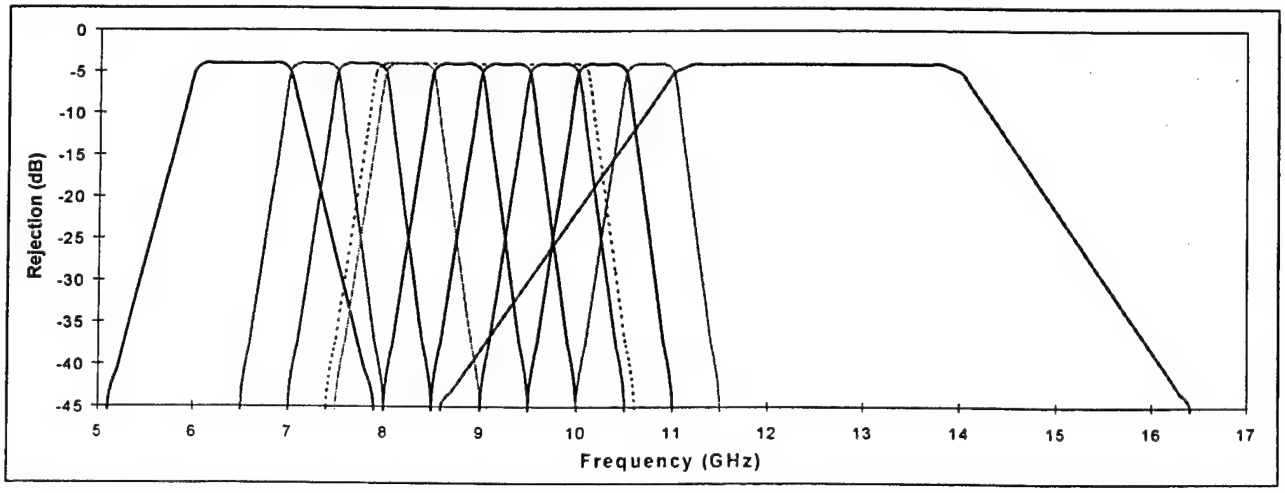

Figure 5.1.1-1. RF Preselect Filter Bands

TABLE 5.1.1.1-1. RF PRESELECT FILTER REQUIREMENTS

Requirement	*Channel*	*Limits*		*Unit*
INPUT SIGNALS				
Input Frequency Band		6 to 14		GHz
Passband Input Return Loss	BPF 1&10	12 min		dB
	BPF2-9,11-12	15 min		dB
RF Input Power	All Channels	2.0 peak 1.0 avg maximum		W
DC Power and Current		See Para. 3.1.3.6 herein		
Digital Control Signals		See Para. 3.1.3.4 herein		
OUTPUT SIGNALS 1/				
		Lower Passband Freq	*Upper Passband Freq*	
Passband Frequencies		F_{PL}	F_{PH}	
	BPF1	5.97	7.03	GHz
	BPF2	6.97	7.53	GHz
	BPF3	7.47	8.03	GHz
	BPF4	7.97	8.53	GHz
	BPF5	8.47	9.03	GHz
	BPF6	8.97	9.53	GHz
	BPF7	9.47	10.03	GHz
	BPF8	9.97	10.53	GHz
	BPF9	10.47	11.03	GHz
	BPF10	10.97	14.00	GHz
	BPF11	8.00	10.00	GHz
	BPF12	7.0	11.0	GHz
Rejection Frequencies		*Lower Rejection Freq*	*Upper Rejection Freq*	
	BPF1	DC to 4.50	8.10 to 15	GHz
	BPF2	DC to 6.22	8.28 to 15	GHz
	BPF3	DC to 6.72	8.76 to 15	GHz
	BPF4	DC to 7.22	9.28 to 15	GHz
	BPF5	DC to 7.74	9.70 to 15	GHz
	BPF6	DC to 8.22	10.26 to 15	GHz
	BPF7	DC to 8.74	10.78 to 15	GHz
	BPF8	DC to 9.22	11.32 to 15	GHz
	BPF9	DC to 9.72	11.82 to 15	GHz
	BPF10	DC to 8.60	N/A above 15	GHz
	BPF11	DC to 6.90	11.10 to 15	GHz
	BPF12	N/A	N/A	
Filter Rejection	BPF 1-11	45 min		dB
Passband Insertion Loss	BPF 4-9	5.5 max		dB
	BPF 1-3, 10-12	6.7 max		dB
3rd Order Input Intercept Point	BPF 1-12	+ 45 min		dBm
Passband Gain Variation	BPF 2-9, 11-12	1.0 max		dB
Passband Sinusoidal Gain Ripple	BPF 11-12	< 0.4 peak-peak for ripple frequency >600MHz		dB
Passband Phase Linearity	BPF 2-9	±5.0 for f±30MHz where $F_{PL}+30 < f < F_{PH}-30$		degrees
Passband Sinusoidal Phase Ripple	BPF 11-12	< 4.0° peak-peak for ripple frequency >600MHz		degrees
Output Return Loss	BPF 1-12	10 min		dB
Analog Power Monitor		See Para. 3.1.3.3 herein		
Switching Speed 2/	All Channels	1.0 max		µs
Recovery Time 3/	BPF1-12	75 max		ns
Noise Figure	BPF1-12	<0.2 dB relative to IL		dB
FM Noise	BPF1-12	See Para. 3.1.3.2 herein		

1/ With the input signal applied to J1, the output signal is measured at J2.

2/ The switching speed shall be measured from the 50% point of the RF Pre-Select input signal to the 90% point of the RF output voltage envelope.

3/ Recovery time shall be defined as the time from the 90% point of the trailing edge of the max signal pulse to the time when the output is within 1dB of the nominal operating insertion loss.

TABLE 5.1.1.1-2. RF PRESELECT FILTER CONTROL SIGNAL FUNCTIONAL REQUIREMENT

Channel Select Control Bits						
ICNTL 4 MSB	*ICNTL 3*	*ICNTL 2*	*ICNTL 1 LSB*	*Channel Name*	*Passband (GHz) (for reference)*	*Comments*
0	0	0	0	BPF11	8.00 to 10.00	High Loss Path
0	0	0	1	BPF12 (Thru Line)	7.00 to 11.00	High Loss Path
0	0	1	0	BPF2	6.97 to 7.53	High Loss Path
0	0	1	1	BIT PWR MON	9.00 to 10.00	High Loss Path
0	1	0	0	Not Used	N/A	
0	1	0	1	BPF4	7.97 to 8.53	Low Loss Path
0	1	1	0	BPF6	8.97 to 9.53	Low Loss Path
0	1	1	1	BPF8	9.97 to 10.53	Low Loss Path
1	0	0	0	BPF9	10.47 to 11.03	Low Loss Path
1	0	0	1	BPF7	9.47 to 10.03	Low Loss Path
1	0	1	0	BPF5	8.47 to 9.03	Low Loss Path
1	0	1	1	Not Used	N/A	
1	1	0	0	BPF1	5.97 to 7.03	High Loss Path
1	1	0	1	BPF3	7.47 to 8.03	High Loss Path
1	1	1	0	BPF10	10.97 to 14.00	High Loss Path
1	1	1	1	Terminated	N/A	High Loss Path

5.1.1.2 RF Preselect Filter Input/Output Signals. The preselect filter contains one RF input port J1 and one RF output port J2. Both RF ports use full detent male SMP or GPO connectors with a characteristic impedance of 50 ohms. All control signals and DC inputs are via 500 pf feed through filter solder terminals. The minimum cutoff frequency is 90 MHz. All digital input signals are required to be single ended Low Voltage (LV) and TTL compatible. The input Voltage Logic 1 is defined as 2.0 V min to 5 V max. The input Voltage Logic 0 is defined as 0V min to 0.8 V max. The maximum input leakage current is 250 μA. The typical usage of this part is Logic 1 = 3.3 V and Logic 0 = 0 V. When the input is disconnected, the Preselect Filter will treat the input as Logic 0. The input and output signals are listed in Table 5.1.1.2-1.

TABLE 5.1.1.2-1 RF PRESELECT FILTER INPUT/OUTPUT SIGNALS

PIN #	*Function*	*Input/Output*
FL1	+3V	Input
FL2	ICNTL 4(MSB)	Input
FL3	ICNTL 3	Input
FL4	ICNTL 2	Input
FL5	ICNTL 1(LSB)	Input
FL6	-8V	Input
FL7	PM Indicator	Output
FL8	+5V	Input
E1	DC Ground	N/A
J1	Analog/RF	Input
J2	Analog/RF	Output

5.1.2 X-Band Downconverter

The X-band downconverter Microwave Integrated Circuit (MIC) converts received RF input signals to an intermediate frequency of 1380 MHz by way of a single down conversion. The MIC incorporates highly integrated multi-function MMICs to achieve cost and size reductions. The MIC provides IF blanking, IF selection, image selection, bandwidth selection, temperature sensing, and power monitors for interference detection. The MIC provides an auxiliary IF input port to support processing an IF input from an external source. The MIC block diagram is shown in Figure 5.1.2-1. The block diagram is not to be construed as prescribing system architecture.

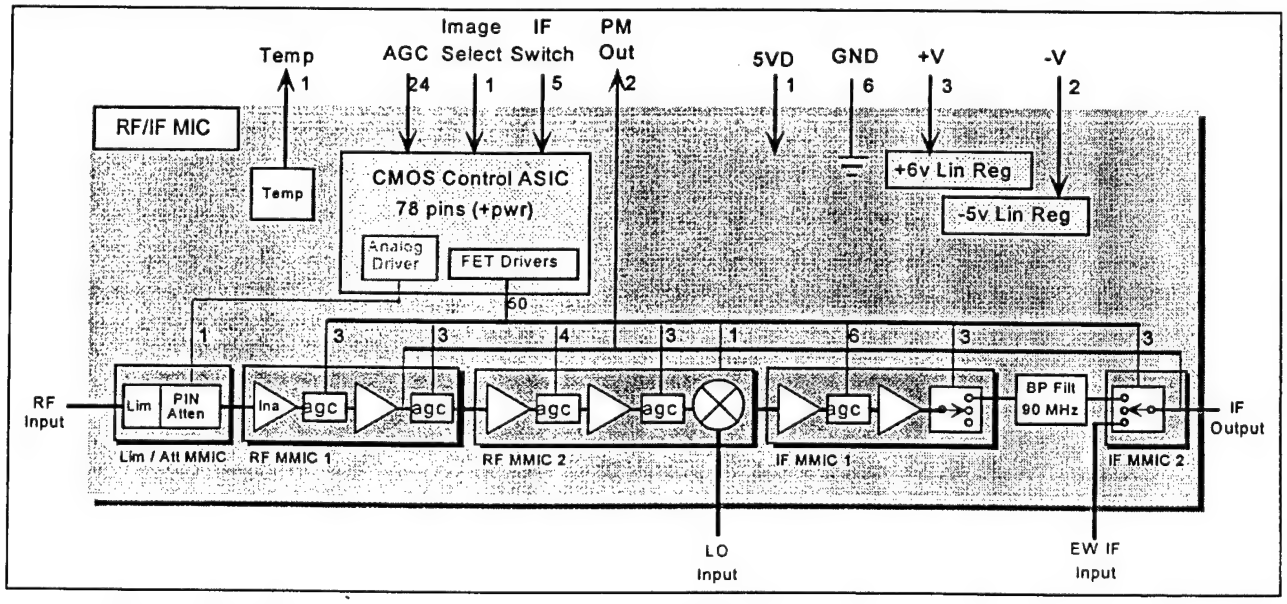

Figure 5.1.2-1 X-Band Downconverter MIC Block Diagram

5.1.2.1 X-Band Downconverter Performance. The MIC provides Automatic Gain Control (AGC) as described in Table 5.1.2.1-1.

The AGC is allocated into compensation AGC and tactical AGC. Compensation AGC is used to compensate for manufacturing process variations (approximately 10 dB), frequency compensation (approximately 5 dB), and temperature compensation (approximately 15 dB). The availability of compensation AGC helps improve manufacturing yields and ensures proper operation over all operating conditions. Approximately 30 dB is allocated to compensation AGC, with the remaining 68 dB of AGC allocated to tactical operation. A limiter is located at the input port to the MIC to protect the following amplifiers and circuit functions from damage due to incident power. The requirements for the limiter are as specified in Table 5.1.2.1-2. The MIC gain, noise figure and Third Order Output Intercept Point shall be per Table 5.1.2.1-3 over the operating temperature range of -40°C to +71°C and over the Extended Band of 6 to 14 GHz given 15 dB maximum of temperature compensation AGC. Third order output intercept point is referenced to two input RF tones separated by 20 KHz with S1 = -45 dBm and S2 = -80 dBm.

The residual phase noise of the device shall be as shown in Figure 5.1.2.1-1 given an RF input power of –20 dBm (-15 dBm – 5 dB) and AGC set to provide an output power of -15 dBm at the MIC output.

TABLE 5.1.2.1-1 AGC COMPENSATION

Function	*AGC*	*AGC Step Size*
Limiter	10 ± 2 dB (7-11GHz), 10 ± 3 dB (6-7 and 11-14 GHz)	10dB step
RF AGC	45 ± 1 dB (7-11GHz), 45 ± 1.5 dB (6-7 and 11-14 GHz)	0 to 16dB in 4dB steps, 17 to 45dB in 1dB steps
IF AGC	43 ± 0.5 dB	1dB steps
Total	98 dB	

TABLE 5.1.2.1-2 LIMITER REQUIREMENTS

Parameter	*Requirement*
Operating Frequency	6 - 14 GHz
Incident Power	+26dBm CW power maximum
Flat leakage	15dBm maximum
Spike leakage	0.3 erg maximum
Recovery Time	< 50 ns to specified insertion loss or AGC

TABLE 5.1.2.1-3 X-BAND DOWNCONVERTER PERFORMANCE PARAMETERS

	6 to 7 GHz	***7 to 11 GHz***	***11 to 14 GHz***
Gain (dB)	55.8 ± 9.0dB	55.8 ± 7.0 dB	55.8 ± 10.0dB
Noise Figure (dB)	5.3	5.0	5.6
Third Order Output Intercept Point (dBm)	17.8	20.8	17.8

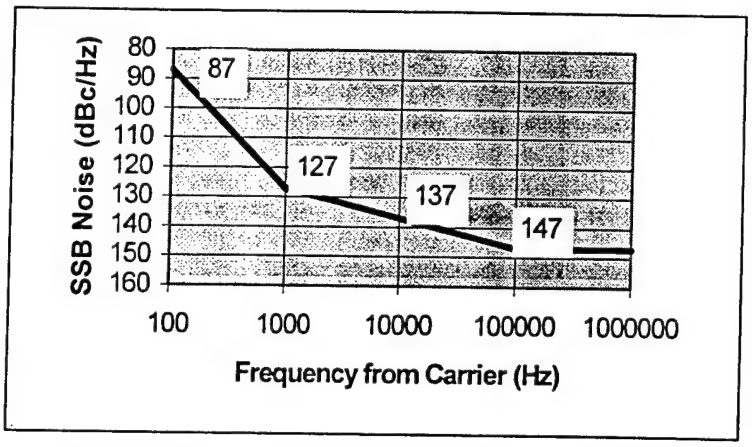

Figure 5.1.2.1-1. Residual Phase Noise

5.1.2.2 X-Band Downconverter Input/Output Signals. The input signals and characteristics are given in Table 5.1.2.2-1. Signal path commands are given in Table 5.1.2.2-2. Output signals and characteristics are given in Table 5.1.2.2-3. The four RF ports have male GPO connectors with a characteristic impedance of 50 ohms. The digital signals operate between +5.0 V and 0 V with the following logic levels:

Logic High (1) VIH = 2.0 V to +5 V, IIH = 250 μA max

Logic Low (0) VIL = 0 V to 0.8 V, IIL = -10 μA max

TABLE 5.1.2.2-1 X-BAND DOWNCONVERTER INPUT SIGNAL CHARACTERISTICS

Signal Name	*Description*	*Signal Type/Characteristics*
RF_IN	Received RF signal	ANALOG FREQ: 6GHz-14GHz PWR: -5 dBm max. operating (+26dBm, CW, max w/o damage.)
LO_IN	Signal for downconversion of RF_IN to an IF frequency	ANALOG FREQ: 6GHz-14GHz PWR: 10.5 dBm ± 2 dB dBm max. operating (+20dBm max w/o damage.)
EW_IF_IN	Received EW IF signal	ANALOG FREQ: 1.38 GHz ± 30 MHz PWR: 0 dBm max. operating 17 dBm max. input no damage
LAGC0-1 (LAGC2-3 ARE RESERVED)	Limiter Attenuator Control	TTL-SE LAGC0 (LIM_VA) LAGC1 (LIM_VB) LAGC2 (LIM_VC) RESERVED LAGC3 (LIM_VD) RESERVED LAGC(1-0) – Atten 01 – 0 dB 10 – 10 ± 2dB 00 or 11 not allowed

Signal Name	*Description*	*Signal Type/Characteristics*
RFAGC 0-12	RF AGC in RFMMIC1, RFMMIC2 Control	TTL-SE Logic 0 attenuation disabled Logic 1 attenuation enabled RFAGC0 (RF1AGC1_1)- 1 dB RFAGC6 (RF2AGC1_1)- 1 dB RFAGC10 (RF2AGC2_1)- 1 dB (±1dB) Logic 0 attentuation enabled Logic 1 attentuation disabled RFAGC1B (RF1AGC1_2)- 2 dB RFAGC2B (RF1AGC1_4)- 4dB RFAGC3B (RF1AGC2_4b)- 4 dB RFAGC4B (RF1AGC2_4a)- 4 dB RFAGC5B (RF1AGC2_8)- 8 dB RFAGC7B (RF2AGC1_2)- 2 dB RFAGC8B (RF2AGC1_4)- 4 dB RFAGC9B (RF2AGC1_8)- 8 dB RFAGC11B (RF2AGC2_2)- 2 dB RFAGC12B (RF2AGC2_4)- 4 dB (±1d)
IFAGC 0-6	Fine AGC in IFMMIC1 Control	TTL-SE Logic 0 attentuation 0dB Logic 1 attentuation enabled IFAGC0 (IF1G0_1DB)- 1 dB IFAGC1 (IF1G1_2DB)- 2 dB IFAGC2 (IF1G2_4DB)- 4 dB IFAGC3 (IF1G3_8DB)- 8 dB IFAGC4 (IF1G4_16DB)- 16 dB IFAGC5 (IF1G5_4DB)- 4 dB IFAGC6 (IF1G6_8DB)- 8 dB (±0.5dB)
IF_BLANK	Controls IF Output MMIC blanking switch	TTL – SE (IF1BLNKA & IF1BLNKB tied together) See Table 5.2.2-2 for characteristics Logic 0 = unblanked **(default)** Logic 1 = blanked
IFMMIC1_WB IFMMIC1_NB IFMMIC2_WB IFMMIC2_NB	Controls the IF Filter selection	TTL – SE See Table 5.2.2-2 for characteristics IFMMIC1_WB (IF1WB) IFMMIC1_NB (IF1NB) IFMMIC2_WB (IF2WB) IFMMIC2_NB (IF2NB) Logic 0 = disabled Logic 1 = enabled
IMG_SLCT	Selects high or low side downconversion in the image reject mixer	TTL – SE (RF2TX2) Logic 0 = low side LO (RF-LO=IF) (default) Logic 1 = high side LO (LO-RF=IF)
EW_SLCT	Selects EW port Input	TTL – SE (IF2EW) See Table 5.2.2-2 for characteristics Logic 0 = EW port disabled (default) Logic 1 = EW port enabled

TABLE 5.1.2.2-2 SIGNAL PATH COMMANDS

IF_BLANK	*IFMMIC1_WB*	*IFMMIC1_NB*	*IFMMIC2_WB*	*IFMMIC2_NB*	*EW_SLCT*	*Signal Path*
0	1	0	1	0	0	WB UNBLANK
0	0	1	0	1	0	NB UNBLANK
1	0	0	1	0	0	WB BLANK
1	0	0	0	1	0	NB BLANK
1	0	0	0	0	1	EW

All other combinations are not allowed

TABLE 5.1.2.2-3 X-BAND DOWNCONVERTER OUTPUT SIGNAL CHARACTERISTICS

Signal Name	*Description*	*Signal Type*
IF_OUT	The downconverted analog IF output signal	Analog Freq: 1380 MHz ± 35 MHz
RFPMOUT	RF power monitor status indicator	Analog
IFPMOUT	1 bit IF par monitor status indicator	Analog
TEMP	Temperature Sensor	Analog

5.1.3 Narrowband ADC

The most significant requirements imposed on a receiver's ADC are instantaneous signal bandwidth and dynamic range. The maximum dynamic range is determined by the need to find low cross section targets in high clutter look down situations. At the other end of the spectrum, the maximum instantaneous bandwidth is dictated by the resolution requirements of surveillance mapping and ground target identification and tracking. The conventional approach to radar receivers shown in Figure 5.1.3-1 is complicated to a large extent by current ADC limitations. At least two downconversions are required, and for good air-to-air performance, analog clutter rejection may be used and require a third downconversion for Doppler tuning. There is no conventional-type of ADC that can satisfy both the worst case signal bandwidth requirements and the worst case dynamic range requirements. Therefore, the conventional solution uses both high-speed low-resolution ADCs and low-speed high resolution ADC's. This approach is complicated, bulky and costly.

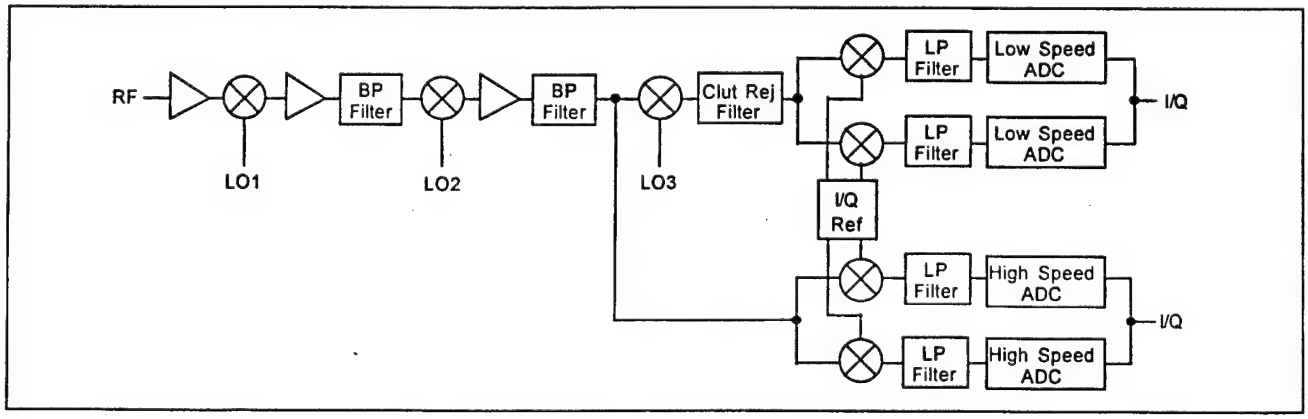

Figure 5.3.1-1. Conventional Analog I/Q Receiver

Improving ADC technology to allow direct IF sampling would significantly reduce the size of radar receivers. Figure 5.3.1-2 shows a radar receiver sampling at the second IF. The conventional receiver in Figure 5.3.1-1 requires 6 mixers and 4 ADCs, whereas the IF sampling receiver in Figure 5.3.1-2 requires only 2 mixers and 1 ADC.

A tunable bandpass Delta-Sigma ($\Delta\Sigma$) modulator allows the use of a single ADC for both wideband and high dynamic range modes. The passband of the ADC can be tuned to the IF of the digital receiver as shown in Figure 5.3.1-3. These bandpass $\Delta\Sigma$ modulators have the property that the ADC resolution, or SNR, increases as signal bandwidth decreases at the IF, effectively allowing bits to be traded for bandwidth.

5.1.3.1 Narrowband ADC Performance Parameters. The noise shaping of the Delta-Sigma Modulator can be adjusted to give optimum performance in both narrowband and wideband modes. This is accomplished by adjusting the poles of the resonators and placing the effective zeros of the noise spectrum at the optimum frequency locations.

The modulator is capable of operation in both narrowband and wideband modes. These mode bandwidths and minimum signal to noise requirements are shown in Table 5.1.3.1-1.

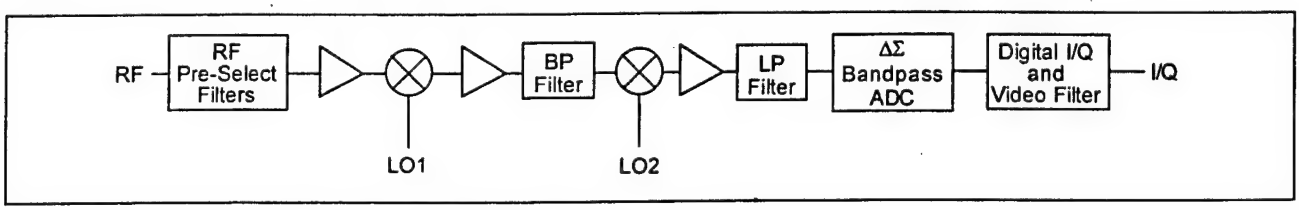

Figure 5.3.1-2. Second IF Sampling Digital I/Q Receiver

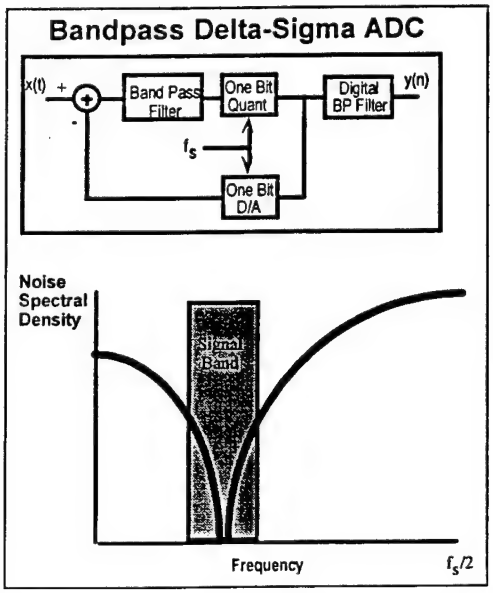

Figure 5.3.1-3. Diagram of Tunable $\Delta\Sigma$ Modulator

TABLE 5.1.3.1-1. NARROWBAND ADC SIGNAL TO NOISE RATIOS

Mode	*Bandwidth*	*Minimum SNR*
Wideband	60 MHz	50 dB
Narrowband 1	7.8 MHz	59 dB
Narrowband 2	2.9 MHz	63 dB
Narrowband 3	1.0 MHz	80 dB
Narrowband 4	0.7 MHz	81 dB
Narrowband 5	0.6 MHz	82 dB
Narrowband 6	0.3 MHz	85 dB

With two tone inputs S1 and S2 which have frequencies in the passband and amplitudes of -6 dBMSA, the third order IMD and all other high order intermodulation products shall be -46 dBMSA for wideband and -88 dBMSA for narrowband. Note that all intermodulation products shall follow classic IMD laws for equal and unequal tones.

With a single tone input S1 having a frequency in the passband and amplitude of -6 dBMSA, all in-band spurs due to harmonic distortion shall be -58 dBMSA for wideband and -99 dBc for narrowband.

With a single tone input S1 having a frequency in the passband, amplitude of -6 dBMSA, and sampled at FS, the SFDR due to spurs other than harmonics of the input tone shall be -73 dBMSA for wideband and -99 dBc for narrowband.

5.1.3.2 Narrowband ADC Input/Output Signals. The input signals and their characteristics are given in Table 5.1.3.2-1. Output signals and their characteristics are given in Table 5.1.3.2-2. DC supply voltages are described in Table 5.1.3.2-3. DC supply currents are described in Table 5.1.3.2-4.

TABLE 5.1.3.2-1 NARROWBAND ADC INPUT SIGNALS

Signal Name	*Description*	*Signal Type/Characteristics*
BASE	Temp Sensing Device Base	Analog Current Input
EMIT	Temp Sensing Device Emitter	Analog Current Return
VIN VINB	IF Input True IF Input False	Differential Pair Center Frequency (FC): 180 MHz nominal Input Frequency Range: FC ± 30 MHz Input Impedance: 200 Ω Maximum Specified Amplitude: ± .65 V peak AC, (MSA) 0 V DC offset Maximum Power: ± 2 V peak AC, (without damage) 0 V DC offset
CK CKB	Input Clock True Input Clock False	50 Ω Differential Frequency: F_S = 3.84 GHz nominal Amplitude (min): ± 80 mV peak AC Amplitude (nominal): ± 150 mV peak AC (differential) Amplitude (max): ± 0.5 V peak AC DC Offset: 0V Phase Noise: < 3.9e-4 rad rms
IT1	Gain Trim Bit1	Analog Bias Current
IT2	Gain Trim Bit2	Analog Bias Current
IT3	Gain Trim Bit3	Analog Bias Current
IT4	Gain Trim Bit4	Analog Bias Current
IDAC1	DAC Trim Bit1	Analog Bias Current
IDAC2	DAC Trim Bit2	Analog Bias Current
IDAC3	DAC Trim Bit3	Analog Bias Current
IDAC4	DAC Trim Bit4	Analog Bias Current

TABLE 5.1.3.2-2. NARROWBAND ADC OUTPUT SIGNALS

Signal Name	*Description*	*Signal Type/Characteristics*
DCout	Input Stage Bias Voltage	DC Voltage
MDAT MDATB	Modulator Output True Modulator Output False	50 Ω Differential Frequency: F_S Amplitude: ± 300 mV peak AC (typical differential) ± 200 mV peak AC (minimum differential) Load impedance: 50 Ω
MDCK MDCKB	Fs Clock Output True Fs Clock Output False	50 Ω Differential skew: < 50 ps (with respect to MDAT)
VCSM	Test Point - Analog Modulator Bias Voltage	DC Voltage -3.9 ± 0.25V
VCASM	Test Point - Analog Modulator Bias Voltage	DC Voltage -2.4 ± 0.25V
VREFM	Test Point - Analog Modulator Bias Voltage	DC Voltage +0.9 ± 0.25V
VCSD	Test Point - Digital Bias Voltage	DC Voltage -3.9 ± 0.25V
VCASD	Test Point - Digital Modulator Bias Voltage	DC Voltage -2.4 ± 0.25V
VCSMD	Test Point - Digital Modulator Bias Voltage	DC Voltage +0.9 ± 0.25V

TABLE 5.1.3.2-3. NARROWBAND ADC DC SUPPLY VOLTAGES

Name	*Type*	*Requirement*	*Goal*	*Absolute Maximum*	*DC Return*
VCCA	Positive Analog	+5.0 ± 0.1 VDC	+5.0 ± 0.25 VDC	+5.5 VDC	GNDA
VEEA	Negative Analog	-5.0 ± 0.1 VDC	-5.0 ± 0.25 VDC	-5.5 VDC	GNDA

TABLE 5.1.3.2-4 NARROWBAND ADC DC SUPPLY CURRENTS

DC Voltage Form	*Nominal Current*	*Maximum Current*
VCCA	245 mA	270 mA
VEEA	450 mA	500 mA

5.1.4 Digital Video Processor

The Video Processor performs the functions of video filtering, I/Q formation, channel balancing, sample timing, pulse response shaping, and sampling for Automatic Gain Control (AGC). The VP receives data from a Delta-Sigma Modulator. The data delayed by a selectable number of sample clock cycles and demultiplexed providing fine control of the effective ADC sample point. The data is then filtered to produce high precision in-phase and quadrature sampled video. The filtering is performed in two stages. The first filter is the Decimation Filter that decimates the data by a factor of 16. The output of the Decimation Filter is processed by I/Q Programmable Video Filters (I/Q PVF) forming the in-phase and quadrature video components. The video filters are highly programmable by means of downloadable coefficients and control parameters, which allow precise channel balancing for applications such as Space Time Adaptive Processing (STAP). Figure 5.1.4-1 depicts the VP as part of a Delta Sigma Analog to Digital Converter.

The VP also includes two AGC circuits (AGC1 and AGC2) and a saturation detection circuit called FL2 Saturation Detection. AGC1 uses outputs of the Decimation Filter or AGC Filter to provide sensed power quantities of wideband data. AGC2 uses outputs of the I/Q filter to provide sensed power quantities of narrowband data. FL2 Saturation Detection provides a count of I/Q data exceeding a programmable threshold. This data can be used to set control parameters for the output processing functions of the VP. AGC1, AGC2, and FL2 Saturation Detection functions operate on data over a programmable number of Filter Program Intervals (FPIs).

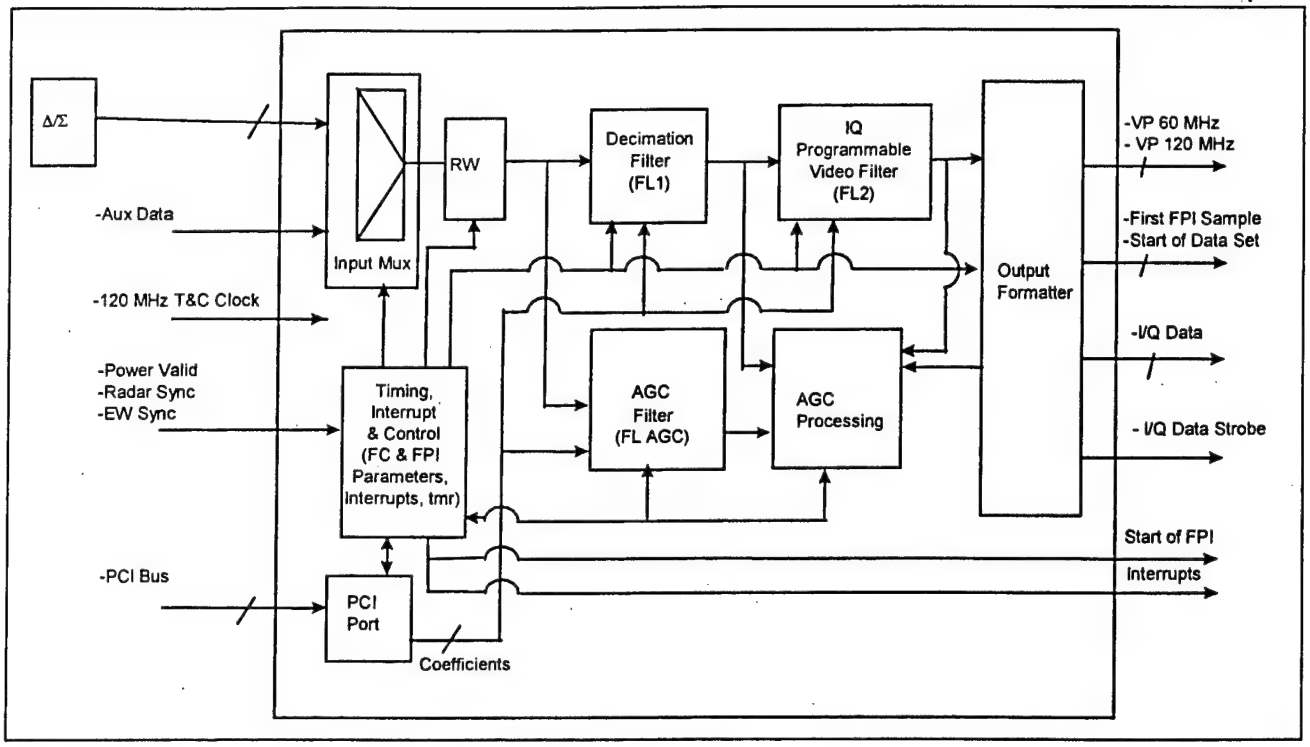

Figure 5.1.4-1. Video Processor Interface Block Diagram

5.1.4.1 Digital Video Processor Performance Parameters. The Video Processor shall receive Filter Cycle (FC) parameters and FPI parameters via a filter coefficient/parameter bus. Decimation Filter data and I/Q Programmable Video Filter coefficients shall be received over this same bus. A Data Type Select signal on the bus shall indicate which one of the four types of data is being communicated to the Video Processor.

The VP shall receive FC and FPI control parameters, configuration parameters, and filter coefficients via the control port and shall be capable of detecting data transfer errors. The VP shall report these error conditions to the VP Controller.

Filter cycle parameters are loaded once per filter cycle. The 16 bits of data and data strobe shall be received at a rate less than or equal to 60 MHz and registered. Upon a Filter Cycle Start, the data shall be registered into a second bank of registers so that the first bank of registers can be reloaded as the second bank is used. If the input registers are not reloaded prior to Filter Cycle Start the old parameters shall be used and an error flag shall be set. Table 5.1.4.1-1 contains Filter Cycle Parameters that are loaded and used by the ASIC not more than once per filter cycle. Provisions shall be made such that 4 sets of filter cycle parameters can be queued (one active and three passive).

TABLE 5.1.4.1-1. FILTER CYCLE PARAMETERS

Filter Cycle Parameters	*Number of Bits*	*Function*
Decimation Filter Coefficient Set (CS0/CS1) FL1 Coefficient Bank Select (F1CS)	1	Selects between two sets of Decimation Filter coefficients
Decimation Ratio (M)	7	Selects decimation ratio of the I/Q PVF
Number of Filter Paths (F)	3	Selects number of filter paths used in Mux mode
Scaling Control	4	Determines the scaling of the I/Q PVF output prior to rounding
Output Word Length	5	Defines number of bits for the I/Q PVF output sample after rounding
Output Packing	1	Enables packing of the I/Q PVF output samples after rounding
Single VF Block Operation	1	Selects which I/Q PVF banks are used
Video Filter Output Configuration	1	Selects between cross-coupled and non cross-coupled I/Q PVF mode
F2CB (FL2 Coefficient Bank Select)	1	FL2 Bank Selection
AFS (AGC Filter Select)	1	Sample Source select for the AGC Filter (FL1 or FL_AGC data)
AGB (AGC Gating Bypass)	1	Selects all samples from PVF (samples gated by collect or all samples from PBF)
AGC1_TH (AGC1_Threshold)	18	AGC_1 threshold value for which odd/even samples exceeding this value shall be counted
AGC2_THH (AGC2 Threshold High)	28	AGC_2 threshold value for which I/Q samples exceeding this value shall be counted
AGC2_THL (AGC2 Threshold Low)	28	AGC_2 threshold value for which I/Q samples less than this value shall be counted
AGC_rep_count (AGC Repeat Count)	8	Number of FPIs over which AGC data is averaged.
AGC_report _enable (ARE)	1	Enables AGC reports to be output.
FL2_BP (FL2 Bypass)	1	Bypasses FL2 function
FL2_SAT_TH (FL2 Saturation Threshold)	20	FL2 Saturation Detection threshold
AGC_DMA_SA (AGC DMA Start Address)	32	DMA start address for AGC reports

Table 5.1.4.1-2 contains FPI Parameters that are used by the ASIC at most once per FPI. Provisions shall be made such that 4 sets of FPI parameters can be queued (one active and three passive).

TABLE 5.1.4.1-2. FILTER PROCESSING INTERVAL PARAMETERS

FPI Parameters	*Number of Bits*	*Function*
Range Walk Select	3	Determines fine sample timing
No. Of I/Q Samples Suppressed (NC - No Collect)	15	Determines number of output samples to suppress
No. Of I/Q Samples Output (C - Collect)	15	Determines number of output samples to pass on to the I/Q Data Buffers.
No. Of Clocks in a FPI	20	Determines length of an FPI in 120 MHz clocks
No. Of Zero Pads	8	Determines number of 120 MHz clocks to pad at the start of an FPI
(EOFC) End of Filter Cycle	1	If set, these FPI parameters define the last FPI in the current filter cycle and I/Q PVF switches to new filter cycle at end of the FPI. If not set, I/Q PVF remains in same filter cycle
External Sync Inhibit	1	Inhibits external synch discrete
FPI Sync Check	1	If set, the wall clock shall be captured at the beginning of the last FPI of a repeat count
Repeat Count	10	Determines the number of times a set of FPI parameters are used
Start Data Set	1	Tags the first I/Q word of the first FPI in repeat group

Commanded chip reset and basic configuration controls are accomplished by setting the appropriate configuration parameters in the VP Chip Reset & Configuration Register. A list of configuration parameters is shown in Table 5.1.4.1-3. Configuration parameters can be updated at anytime and are effective on the very next clock.

TABLE 5.1.4.1-3. CONFIGURATION PARAMETERS

Configuration Parameters	*Number of Bits*	*Function*
Reset	1	Chip commanded reset
PTM (Pass Through Mode)	1	Configures chip to route data from the input mux directly to the I/Q output ports.
AuxSel (Aux Data Select)	1	Selects 16 bit/240MHz data from the CDR or 32bit/120MHz data from the Aux Data Mux
BPDEC (Bypass Decimation Filter)	1	Configures chip to route data from the input mux directly to the inputs of the I/Q PVF
XSE (External Sync Enable)	1	Enables the VP External Sync Discrete to start a new Filter Cycle
XSS (External Sync Select)	1	Selects which VP External Sync Discrete shall be used. XSS = 0, selects Radar Ext. Sync XSS =1, selects EW Ext. Sync

5.1.4.2 Digital Video Processor Input/Output Signals. The VP receives either 16 bits of data, or 32 bits of auxiliary data from an auxiliary demux. This input data is processed and output as 20 bits of filtered inphase and quadrature digital video along with an I/Q data strobe, a VP clock, a Start of FPI flag, and a Start of Data Set flag.

In addition to the filtered I/Q data, sensed power quantities (i.e. peaks, sums, and counts) from AGC1, AGC2, and the FL2 Saturation Detection circuits shall be output via the control port or PCI bus for further AGC processing.

The VP also receives Filter coefficients for the AGC, Decimation and I/Q Programmable Video filters, Filter Cycle (FC) parameters, and Filter Processing Interval (FPI) parameters as 32 bit data via the PCI bus.

The VP receives timing and control discretes which include two External Syncs (a Radar Sync and an EW Sync) and a Power Valid signal used by the VP's Timing and Control function. The Built in Self Test (BIST) function within the VP communicates via an IEEE 1149.1 Bus with control lines consisting of Test Mode Select, Test Clock, Test Data In, Test Data Out, and Test Reset.

The VP also sources three interrupt signals to its controller.

A list of input and output signals is shown in Tables 5.1.4.2-1 and 5.1.4.2-2, respectively.

TABLE 5.1.4.2-1. VIDEO PROCESSOR INPUT SIGNALS

Signal Name	*Source*
Test Mode Select	Test Controller
Test Clock	Test Controller
Test Data In	Test Controller
Test Reset	Test Controller
VP Tristate Enable	Hardwired
LVDS Reference Voltage In	Hardwired
Aux Data (31:0) T, F	Aux Demux
Aux Data Receiver Power Down	Hardwired
T&C Clock T, F	System T&C
Mod Data (15:0) T, F	CDR
Mod Data Receiver Power Down	Hardwired
Clock T, F	CDR
PCI Bus Clock	VP Controller
PCI Reset Not	VP Controller
PCI Inititalization Device Select	VP Controller
PCI Grant Not	VP Controller
Ext Sync (Radar, Default) T,F	System T&C
Ext Sync (EW) T,F	System T&C
Power Valid	Power Supply
I/F Select	Hardwired

TABLE 5.1.4.2-2. VIDEO PROCESSOR OUTPUT SIGNALS

Signal Name	*Destination*
Test Data Out	Test Controller
VP Output Clock T, F	I/Q Data Buffer
I Filtered Data (19:0)	I/Q Data Buffer
I Data Saturated	TBD
Q Filtered Data (19:0)	I/Q Data Buffer
Q Data Saturated	TBD
I/Q Data Strobe T, F	I/Q Data Buffer
Start of FPI	I/Q Data Buffer
First Sample in FPI	I/Q Data Buffer
Start Data Set	I/Q Data Buffer
Decimation Filter Overflow	TBD
VP Interrupts	VP Controller
PCI Interface	VP Controller

5.1.5 Embedded Controller

The Embedded controller (EC) is a general purpose computer designed to be used as an embedded control element in the modular RF System. In addition to the narrowband receiver controller application, the EC will be reused in other modular RF system applications such as the Beam Steering Computer general purpose processor, power supply controller and Sensor Hardware Encapsulation Layer (SHEL) controller.

The EC is comprised of a microprocessor, memory, and peripheral interfaces as shown in Figure 5.1.5-1. The EC is a functional building block, as defined in Section 3, made up entirely of COTS parts and exists as a reference design that can be included on a host multilayer printed wiring board along with other RF building blocks.

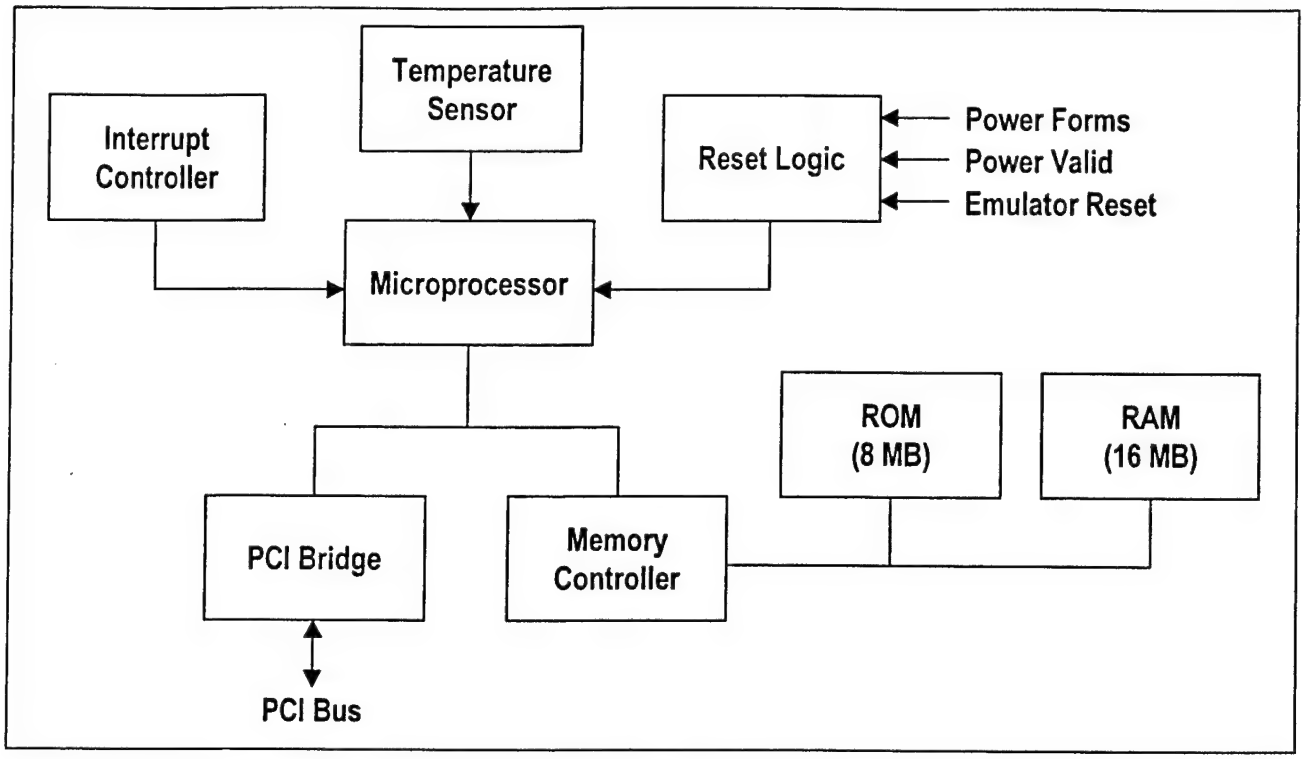

Figure 5.1.5-1. Embedded Controller Functional Block Diagram

5.1.5.1 Embedded Controller Performance. The heart of the EC is a microprocessor having the following capabilities:

- It shall support clock rates between 180 MHz and 266 MHz
- It shall execute 32 bit fixed point instructions with a SPECint95 of 6.6 @ 266 MHz
- It shall execute floating point instructions with a SPECfp95 of 5.5 @ 266 Hz and handle IEEE-754 single and double precision data types

The EC shall support a 32 bit PCI bus (PCI Local Bus Specification Rev 2.1) at clock rates up to 66 MHz and provide arbitration for up to 5 bus masters.

The EC shall have at least 16 Mbytes of RAM and 8 Mbytes of ROM that is loadable over the PCI bus. The memory controller shall support microprocessor memory burst read/write operations over the PCI bus. Writes to the ROM boot block shall be inhibited unless a ROM write enable input is true

The interrupt controller shall accept 15 independent external interrupts and 8 multiplexed external interrupts. The interrupts shall be individually maskable under microprocessor program control. The microprocessor shall provide up to 16 interrupt priority levels that can be uniquely assigned to the independent interrupts under program control and assigned to the multiplexed interrupts as a group also under program control.

The EC shall include a temperature sensor that can be mounted on the host module PWB. The temperature sensor shall have an accuracy of ± 2°C and cover the range of 25 to 100°C.

The EC shall only require 2.5V and 3.3V power forms and shall consume less than 6 W. The reset logic function provides voltage supervision and power sequencing functions for the EC and the host module. The reset logic shall monitor the 3.3V and 2.2V and an external power valid signal and provide a reset to the microprocessor and host module if the power forms are out of range or power valid is not true. The reset logic shall also reset the microprocessor when it receives an emulator reset signal.

The EC shall include an IEEE 1149.1 interface for test access and emulator support.

The EC shall take up less than 10 square inches of board area when laid out on a multilayer PWB with at least 6 signal layers.

5.1.5.2 Embedded Controller Input/Output Signals. The EC interface signals are listed in Table 5.1.5.2-1.

5.2 SUITABILITY FOR USE IN AIR-TO-GROUND RECONNAISSANCE SYSTEMS

5.2.1 Introduction

Reconnaissance radars typically have one or both of two operating modes: Synthetic Aperture Radar (SAR) and Ground Moving Target Indication (GMTI). Fine resolution, large coverage SAR is a driver of the receiver subsystem, especially of the analog-to-digital conversion (ADC) building block. The ADC will, therefore, be the focus of this section.

SAR imposes two conflicting requirements on the ADC. Quantization noise is an important component of the SAR image quality error budget. The particular implementation of the ADC function employed by the receiver complicates quantization noise modeling for SAR since the noise is colored (varies with frequency). For common high resolution SAR implementations, this causes the signal-to-quantization noise ratio to be vary with range in the image.

The second requirement is derives from a linear relationship between the SAR range coverage and the IF bandwidth of the radar. As the coverage grows so must the IF bandwidth. But as the IF bandwidth grows, so does the quantization noise. Complicating this is the fact that

TABLE 5.1.5.2-1. EMBEDDED CONTROLLER INTERFACE DESCRIPTION.

EC Interface Signal	*Description*
PCI Bus	32 bit PCI that complies with PCI Local Bus Specification Rev 2.1, max clock rate 66 MHz
Independent Interrupts	15 maskable interrupts - priority can be assigned independently
Multiplexed Interrupts	8 maskable interrupts – priority assigned as a group
ROM Write Enable	Enables programming of the ROM boot up blocks
Power valid	Holds microprocessor in reset state and provides global reset to host module
JTAG port	Complies with IEEE 1149.1
Emulator Reset	Resets microprocessor
Module Reset	Reset output for use by host module

after the digital IF is formed the sampling rate is reduced to avoid heavy oversampling and having to deal with the very high data rate resulting from heavy oversampling. The aliasing that results also degrades image quality and must be controlled.

In this section we flow down coverage and image quality requirements to the ADC function. We begin with a discussion of image utility and the philosophy of how the image quality of reconnaissance SARs is specified. A notional specification for quantization noise and digital aliasing is established. Then we show how IF bandwidth and coverage are related. We conclude with requirements for IF bandwidths over which the image quality specifications must be met, and a brief discussion of the future.

5.2.2 Image Utility and Image Quality Specifications

Ideally, image quality would be specified and the SAR would be commanded to produce imagery that could be exploited to achieve a particular purpose. Towards this end a rating scale of radar image utility has been established. The Radar National Image Interpretability Rating Scale (RNIIRS) is modeled on a similar scale developed for optical imagery. The RNIIRS uses a numerical scale from 1 to 9. The integer levels of the scale are defined in terms of the utility of the imagery to allow image analysts to perform specific tasks of interpretation. Thus, by presenting imagery to image analysts, the RNIIRS rating of the imagery can be determined.

Image analysts can be employed in studies to relate specific radar parameters to image utility as defined by RNIIRS. Over the years such studies have allowed the derivation of an image quality equation (IQE) relating transmitted bandwidth (which determines range resolution), collection angle (determining azimuth resolution), range, azimuth and elevation to image utility. For example, for large mapping squint angles from the velocity vector, RNIIRS 6 corresponds to about a resolution of 1 foot for typical SAR processing.

To be useful to radar design engineers, however, the IQE must be extended as shown in Figure 5.2.2-1 to include radar contributors to image quality degradation, or at least to a variety to levels of additive and multiplicative noise. Unfortunately, this has never been done due to the complexity of collecting imagery over all geometries and resolutions with varying noise levels.

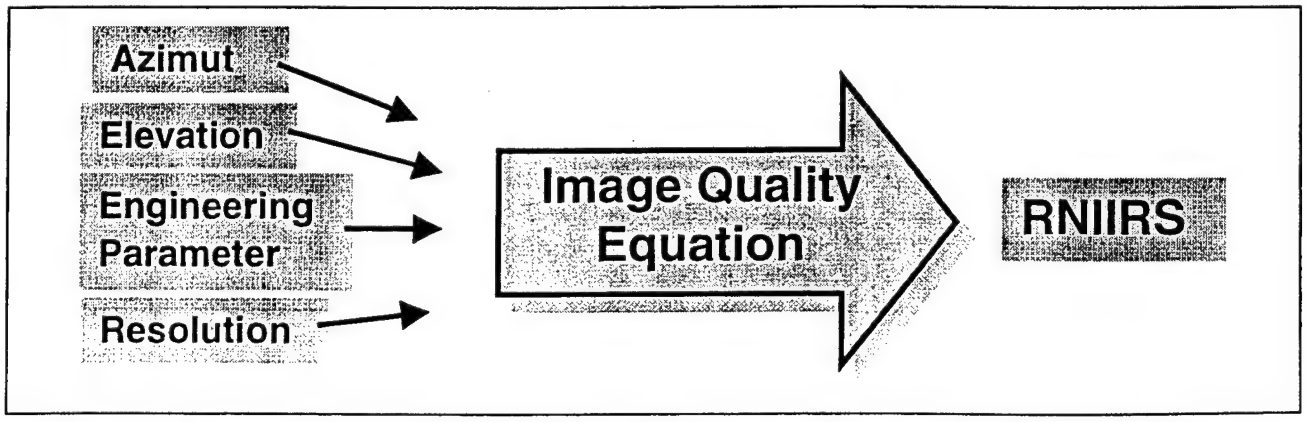

Figure 5.2.2-1. Illustration of an Image Quality Equation Relating SAR Parameters To Image Utility. In theory any engineering parameter (such as additive noise level) could be included. In fact, no engineering parameters are included in the current IQE.

Some limited studies have been done. During the development of the F/A-18 RECCE radar, McDonnell-Douglas artificially inserted multiplicative noise into imagery of one specific resolution and studied the effects on utility. But, to date no IQE exists which relates multiplicative noise, resolution and mapping geometry to RNIIRS. The existing IQE relates resolution and mapping geometry to RNIIRS for a single radar.

The best one can hope to do under these circumstances is to specify a radar under development to achieve image quality comparable to the one for which the IQE exists. This way the IQE will predict utility for the new radar as well. This is the philosophy we are following in specifying radars for image quality.

5.2.3 Specifications for Image Quality

A number of specifications are placed upon a SAR to assure high quality imagery. These specifications are placed upon the SAR impulse response in terms of parameters that can be measured in the imagery itself. The impulse response is the response of the SAR system to a point target. Reference Figure 5.2.3-1 for an impulse response example.

The following specifications are flowed down to specifications on the radar hardware, motion compensation and signal processing in terms the designers will understand:

- Resolution: Since resolution is typically inversely proportional to range coverage several resolutions are usually required. The finest resolution needs to be chosen to provide the utility required to achieve a given mission. The utility required is a mission level requirement. A radar that is required to achieve RNIIRS 6 might have modes with resolutions of 0.3 m, 1.0 m, 3 m and 10 m. The receiver must have adequate front end bandwidth to pass a high resolution waveform.
- Peak Sidelobe Envelope: Placing an envelope over the sidelobe region restricts the peak sidelobes. The far sidelobes are restricted to be less than nominally –35 dB below the

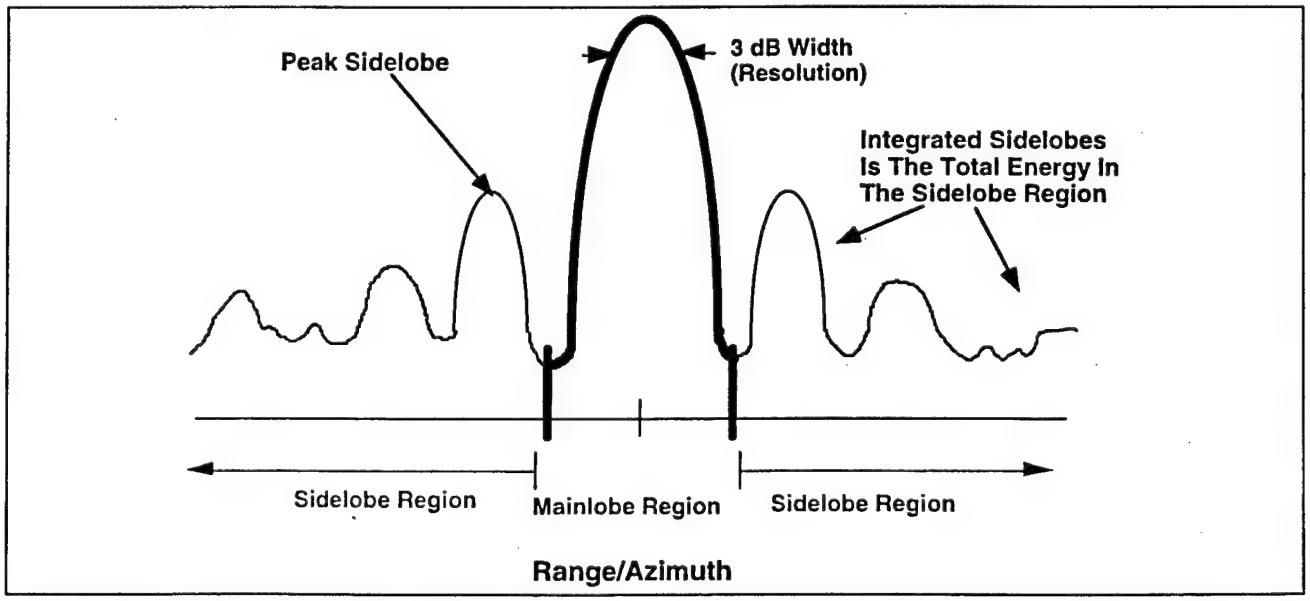

Figure 5.2.3-1. Impulse Response Example. Several aspects of the SAR impulse response are specified, including the 3 dB width (resolution), peak sidelobes and total sidelobe energy.

mainlobe peak. Near sidelobes may rise higher. Front-end filter ripple in the receiver must be controlled to meet this specification. It is not a driving specification.

- Multiplicative Noise Ratio (MNR): Multiplicative noise is noise that is proportional to the signal strength. It behaves much as does dirt on an automobile windshield as the car is approaching oncoming headlights. The signal spreads out everywhere causing there to be little contrast. Multiplicative noise has three components: integrated impulse response sidelobe ratio is the total energy in the sidelobes divided by the total mainlobe energy, quantization noise includes both the noise introduced by the quantization process and the clutter aliased by filtering and resampling operations in the processor, and clutter aliasing due to the pulsed waveform. Multiplicative noise is difficult to control, and the multiplicative noise specification is often a driving specification. ADC quantization noise and clutter aliasing due to resampling the signal are important specifications for the receiver. They should contribute less than –30 dB to the MNR budget.
- Equivalent Noise Reflectivity (ENR): ENR is a radar independent way of specifying the acceptable amount of additive noise in the imagery. When a clutter model is specified, ENR is equivalent to a clutter-to-noise ratio specification. This is not an important spec for the receiver.
- Spurious Responses: Spurs correlated to the signal must be controlled. Careful design of the receiver/exciter frequency plan is the key to meeting this spec. It is not a driver, in general.
- Uncompensated Image Intensity Variation: As this applies to the receiver, the transfer function of the back end filters must be known to within about one dB. In general, the filter supplier's tests are adequate for calibration.

Clearly, the biggest concern when applying the MODRFS receiver to SAR is the ADC function quantization noise and clutter aliasing. This will be discussed in detail below.

5.2.4 The Linear FM Waveform

For many reasons the linear FM (LFM) waveform is the waveform of choice for fine resolution SAR applications. The waveform bandwidth required to meet fine range resolution requirements can be quite large. For example, RNIIRS 6 requires about 600 MHz. If such resolutions are not required, the receiver can pass the entire signal bandwidth to the signal processor where matched filter processing is performed to compress the pulse. In this case the analysis applied to air-to-air waveforms applies, and the fact that for the MODRFS receiver quantization noise varies with frequency is uninteresting.

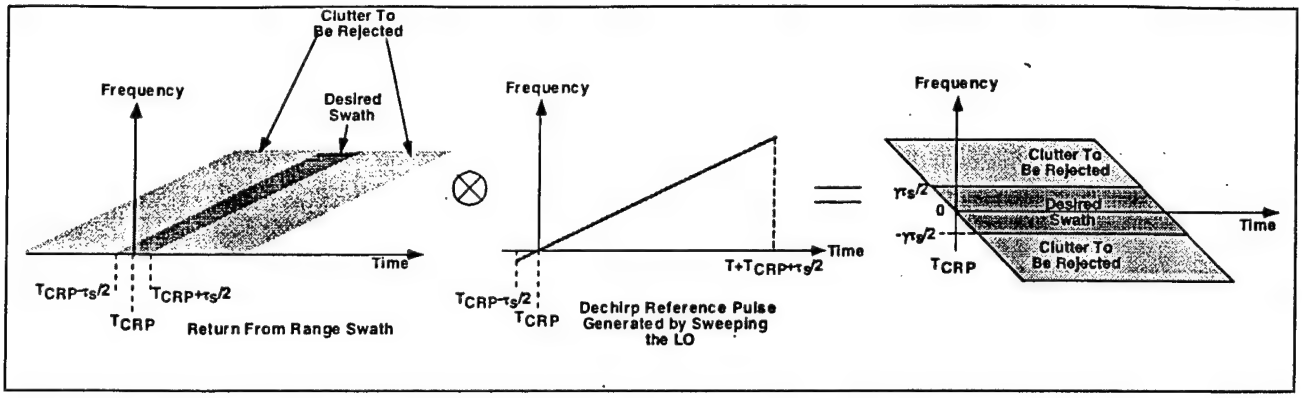

Figure 5.2.4-1. Large Bandwidth LFM Waveform Processing. The returning signal is demodulated by mixing it with the LO modulated to match the return expected from a point near the center of the range swath. If the desired range swath is small, this operation reduces the IF bandwidth required to pass the signal.

For vary large waveform bandwidths, the LFM waveform can be demodulated at RF as part of the first IF downconversion, as illustrated in Figure 5.2.4-1. In many cases, this avoids large IF bandwidth requirements that can place serious demands upon the ADC function.

On the other hand, the demodulation processing causes scatterers at different ranges to appear at different frequencies. The size of the desired swath now drives the IF filter bandwidth requirements. Simply put, a large image coverage requirement can drive the IF bandwidth to be quite large. This is illustrated in Figure 5.2.4-2, where the IF filter bandwidth requirements are plotted as a function of the range coverage requirement for RNIIRS 6 (1 foot resolution) assuming a 100 microsecond pulse width. Expected coverage requirements for tactical systems and for theater and national reconnaissance systems are indicated as well.

5.2.5 Flow Down of Image Quality Requirements to the Narrowband Receiver

After the demodulation processing, clutter outside the desired swath is rejected by the IF filter. In the MODRFS receiver, the IF filter is formed in the preprocessor following the Delta/Sigma modulator. The signal is decimated following the filter in order to reduce the data rate. Two kinds of interference are introduced by this kind of processing: aliasing of the residual clutter passed by the IF filter and quantization noise. This is illustrated in Figure 5.2.5-1. Both of these are considered multiplicative noise. The signal-to-interference ratio is specified to be 30 dB or better.

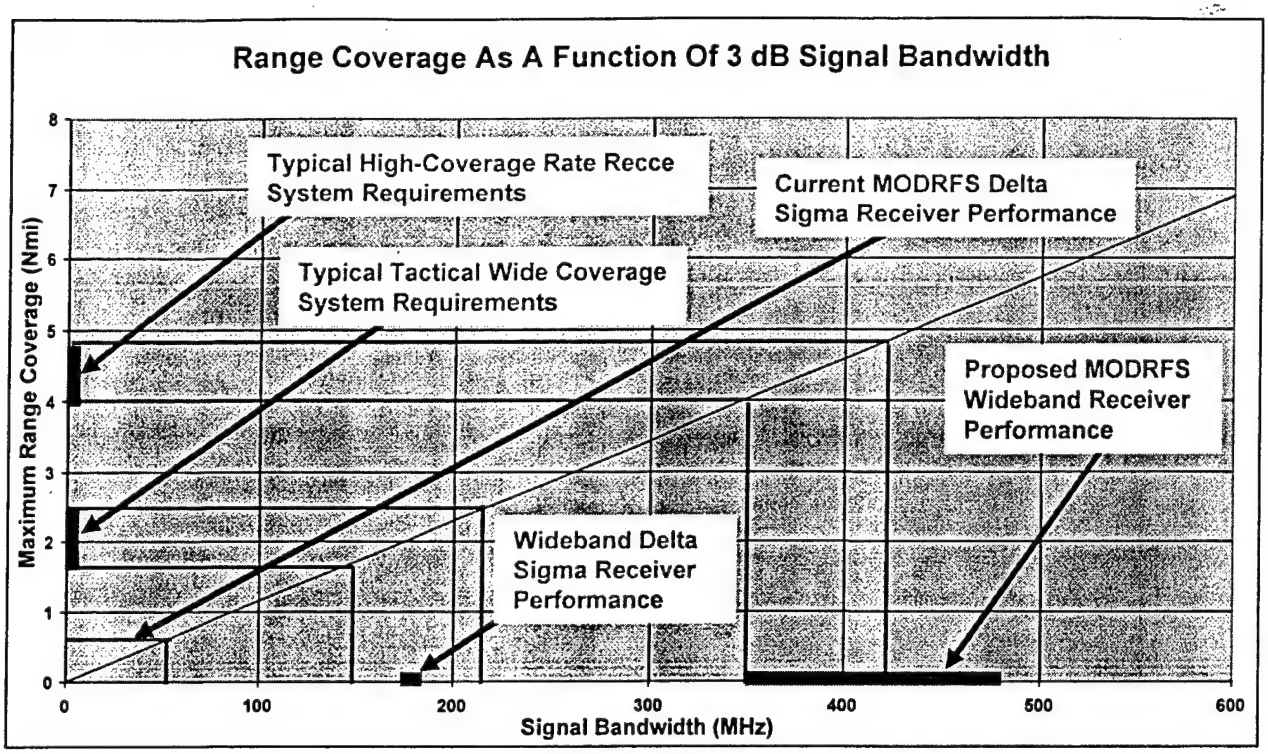

Figure 5.2.4-2. Range Coverage Is Related To IF Bandwidth. The graph shows how range coverage is related to IF bandwidth for an LFM waveform with 600 MHz of bandwidth and a 100 microsecond pulse that has been demodulated at RF.

However, the flow down of the multiplicative noise requirement is complicated by the fact that both the aliasing noise and the quantization noise are colored. That is, they are a function of frequency and hence of range in the image. Reference Figure 5.2.5-1.

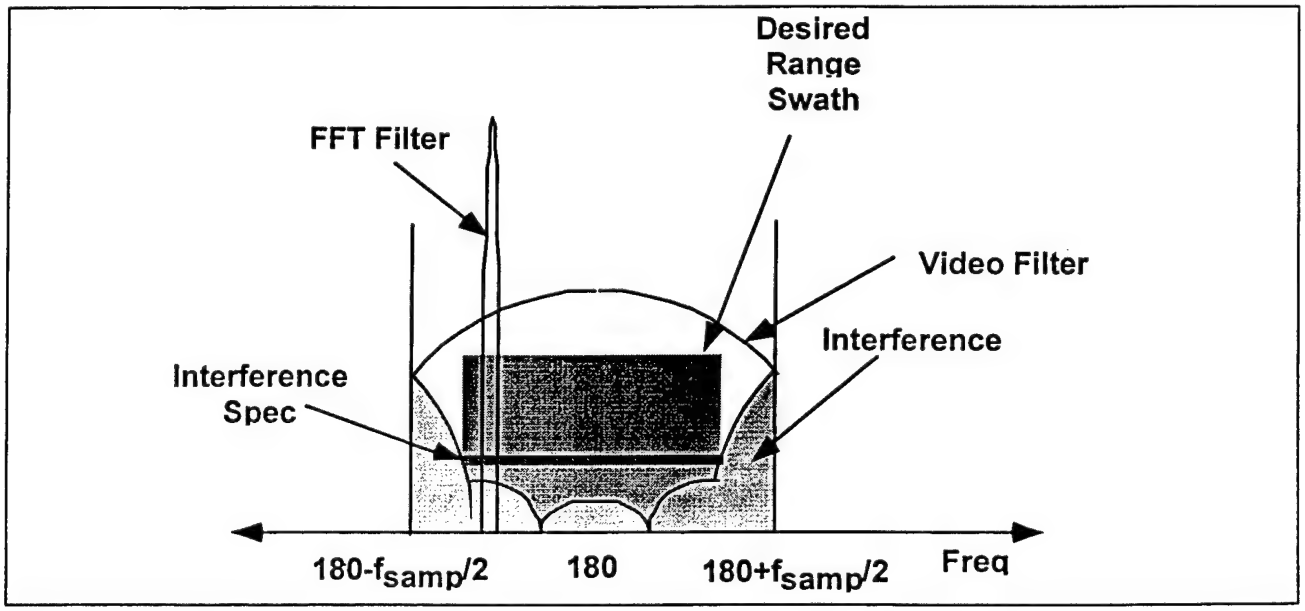

Figure 5.2.5-1. Signal and Interference as a Function of Frequency. Signal-to-Interference ratio is a function of the location in the image, i.e. it is spatially variant. The conservative approach to specifying the MNR is to require the MNR to be better than a fixed level everywhere in the image.

In essence the processing of the LFM waveform is a Fourier transform. This processing isolates the spatial frequencies corresponding to different ranges. Each FFT filter will have a different SNR. Taking a conservative approach, we propose to specify that the signal-to-interference ratio should be better than a fixed level (say 30 dB) everywhere in the image. This is also illustrated in Figure 5.2.5-1.

5.2.6 The Roadmap for the Future

The current generation MODRFS receiver, using a single delta sigma A/D converter in each receiver channel, will support advanced air-to-air and air-to-ground mode suites required by current and next generation fighters. The limited IF bandwidth due to increased quantization noise will constrain the maximum one foot resolution SAR range coverage to about 0.5 nmi. This is more than adequate for a tactical application where the radar operator interprets the imagery. The future applications of tactical SAR, however, may involve cueing of a shooter aircraft to a target by battlefield and national surveillance assets. For this application, wide range coverage (1 to 2 nmi) is desired since a mobile target may have moved since surveillance data was collected. Analysis of an image this large in the cockpit of a fighter aircraft is impossible, so automatic target cueing algorithms become a requirement as well.

As is shown in Figure 5.2.4-2, it is expected that the requirements for wide coverage tactical SAR coverage can be met with a wideband Delta Sigma modulator based MODRFS receiver. However, very wide coverage reconnaissance SAR systems place very stressing requirements upon the receiver design. In the long term, a Delta Sigma modulator based MODRFS receiver may meet these requirements, however, in the short term, other solutions exist. A commercial high speed, high dynamic range flash ADC could be added to the MODRFS receiver to perform the reconnaissance SAR function.

5.3 SUITABILITY FOR USE IN CNI SYSTEMS

The primary CNI functions that were considered candidates for influencing the definition of MODRFS building blocks were the Joint Tactical Information Distribution System (JTIDS) function, and Identification Friend or Foe (IFF) Transpond and Interrogate functions. Key receiver requirements for implementation of these functions are listed in Table 5.3-1.

TABLE 5.2-1. CNI RECEIVER REQUIREMENTS

Parameter	*JTIDS Requirement*	*IFF Transpond Requirement*	*IFF Interrogate Requirement*
Sensitivity	-95 to 0 dBm while operating in the presence of IFF Interrogate or Transpond signals and TACAN interrogate signals	-77 to -22 dBm while meeting a 90% Probability of Detections Sufficient to Initate Reply	-81 to -21 dBm while meeting a 95% Probability of Correct Target Reports for Target Reply Bursts
Pre-Conversion Center Frequency Range	969 to 1206 MHz	1030 +/- 0.05 MHz	1090 ± 0.5 MHz
Detection Bandwidth	5 MHz at 3 dB points	6 MHz at 3 dB points	7.6 MHz at 3 dB points
Selectivity Bandwidth	50 MHz at 3 dB for interfering signal strength of -25 dBm, 400 MHz for interfering signal strength of -10 dBm	24 MHz at 40 dB points, 44 MHz at 90 dB points	11.4 MHz at 3 dB points, 19 MHz at 40 dB points, 50 MHz at 70 dB points
Commandable Attenuation	As needed to support other system performance parameters	As needed to support automatic adjustment of threshold for suppressing effects of interference or jamming, rate not specified	1 dB steps in 2.5 microseconds
Noise Figure	Adequate to meet required Probability of Detections Sufficient to Support Link Symbol Error Rate (classified requirement)	Adequate to meet a 90% Probability of Detections Sufficient to Initiate Reply, and Sufficient False Detections to Trigger Reply Initiation of not more than once in 1 minute	Adequate to meet a 95% Probability of Correct Target Reports for Target Reply Bursts, and a Target False Alarm Reports rate of not more than 1 per 10 seconds
Frequency Following	Receive train tuning and/or receiver switching sufficient to support commanded 13 microsecond waveform frequency hop rate over entire Pre-Conversion Center Frequency Range	Not Applicable	Not Applicable

While the MODRFS narrowband receiver building blocks could possibly be designed to meet these CNI requirements in addition to the requirements of a multifunction radar, it would not be economical to do so. The requirements of the two types of systems are significantly different and an attempt to develop building blocks useable by both systems would likely result in increased component size and cost. In contrast, the telecommunications industry is experiencing tremendous growth and making significant investments in the development of affordable components for low band frequencies. It would be more economical for CNI systems to pursue the use of modular building blocks developed by the telecommunications industry.

6. TRADE STUDY SUMMARY

6.1 CRITICAL INTERFACES

The Multi-Role Fighter Sensor System shown in Figure 4-1 has a number of interfaces of various types. The RF signal, reference and clock distribution, and timing sync and strobe interfaces are more or less dictated by the electrical characteristics of the signals they carry. The remaining data and control interfaces can be handled by two special interface types: digital module data and control, and analog/RF module control. These interface types are further defined in the following sections.

6.1.1 Digital Module Data and Control Interface

Ideally, the digital module data and control interface should have the following characteristics:

- High bandwidth, low latency
- Long haul capability (10 to 15 meters)
- Support point-to-point, network, and bus interconnect topologies
- Suitable for avionics environment
- Commercial support for components, switches, software, tools, etc.

Today these requirements can best be met with Fibre.Channel. It is important to note that commercial standards do have a finite useful life span and tomorrows answer will most likely be different. By placing isolation layers at key interface boundaries, the modular RF system concept will localize the effect of an interface change, making use of a commercial standard more acceptable. The Fibre Channel arbitrated loop topology can be used to emulate a backplane bus (for example, when tying multiple preprocessor modules together). The downside of this is that failure of any terminal on the loop will take down the entire loop. This weakness can be mitigated by routing the Fiber Channel through a reconfigurable hub, thereby preserving the system's tolerance to a receiver channel failure.

6.1.2 Analog/RF Module Control Interface

The requirements for the analog/RF module control interface are even more specialized than the digital module data and control interface. Key characteristics are summarized below:

- Primary function is to serialize discrete control signals
- Command actuation is externally controllable
- Low protocol overhead which does not require microprocessor support
- Minimum use of board area - ideally fits in corner of an FPGA
- Gated clock
- Clock frequencies compatible with the system frequency plan
- Externally controllable data flow

The starting point for identifying a potential open system architecture (OSA) uniform control interface for RF modules was the Common Interface Unit (CIU) developed by the Integrated

Sensor System (ISS) program. The CIU was designed to be a functionally flexible, moderate data rate, digital control interface located on each RF and digital module in the system. Each CIU is identical and controls input/output signals to/from the module hardware. CIUs use lookup tables to obtain specific information on controlling the module on which they are mounted. Incorporation of new assets into the system becomes relatively easy, requiring a CIU with an appropriate software load to be resident on the hardware.

Figure 6.1.2-1 illustrates the CIU concept features which have been specifically designed to handle all of the interface requirements for any RF and digital module types that could be resident in a multifunction RF subsystem. One of the key functions the CIU was required to support for the ISS concept was to interleave module function usage between two or more operational threads in a millisecond time frame. This requirement was met by supplying an accurate clock to the CIU, providing buffer space to hold a cue of commands, and using a command format that included (optionally) a time to execute for each command with an accuracy of 50 nanoseconds.

Using this understanding of the CIU, many of the RF system control design drivers and implementation concepts were reexamined. Key areas of reexamination, along with recommended deviations from the ISS approach, are described below:

- cost, size, and weight allocations for various RF and digital functions
  - **deviation** (from ISS): allocate less board space and cost to module digital interfaces to minimize total number of modules required and overall cost
- on-module clock signal to RF signal isolation capabilities

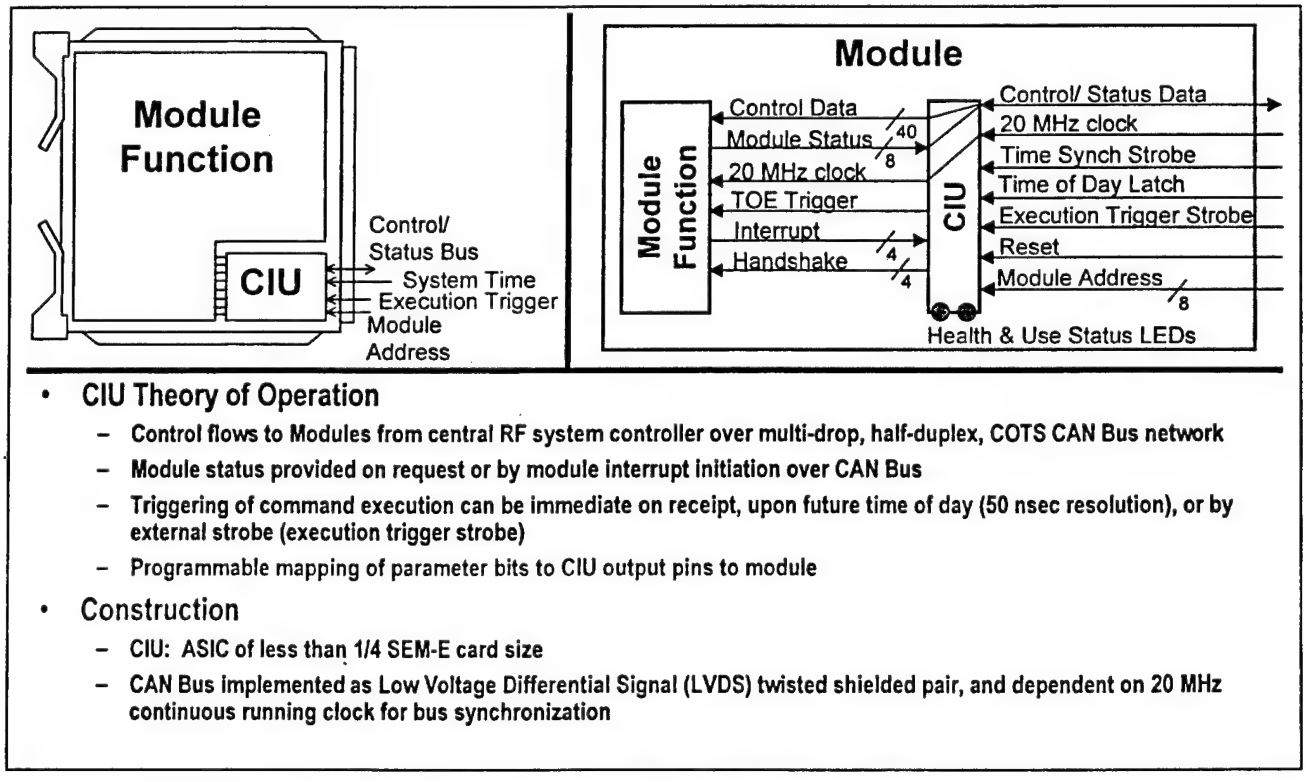

Figure 6.1.2-1. Common Interface Unit (CIU) Concept Overview

- **deviation**: assume (from ISS test results) that perfect isolation is elusive

- module sharing requirements
  - **deviation**: sufficient to normally share on task completion boundaries instead of normally on millisecond by millisecond interleaved basis
- module obsolescence and technology roll upgrades concepts
  - **deviation**: assume module replacements will typically occur in groups and ripple up to affect module controller (direct controller for module being replaced) vs. individual module replacements with no effect on module controller
- allocations of modules to digital networks
  - **deviation**: concept to group modules into subnets based on necessary functional interactions between group members and provide connect points between groups as needed vs. put all modules on universal access digital network

The last area of reexamination, allocations of modules to digital networks, provided the framework for repartitioning of interface requirements into RF module control interface requirements and digital signal (preprocessor/controller and processor/command) module control interface requirements. The other areas of reexamination provided the impetus and substance of what the differences would be in interface requirements for the different module types.

The revision of the requirements led to different design concept solutions for the RF module types versus the digital signal module types. Fibre Channel, as described in the previous section, was selected as the digital signal module interface solution. For the RF module interface solution, the Serial RF Control (SRFC) bus, which is a derivative of an F-22 RF control bus, was selected.

The digital signal modules interface solution selection was partly driven by the efficiency of using the same high data rate interface for control as was needed for signal data output. The signal data output bit rates were orders of magnitude higher than that required for control purposes but the resulting data interface provided a convenient return path that could handle all control data.

The RF modules, on the other hand had two very different requirements. One was to receive real-time low latency control data from pre-processor/controller modules performing high speed control logic and parameter calculations while at the same time generating minimal on-module noise (by minimizing on-module data clock signals).

The SRFC was designed to be a functionally flexible, moderate data rate, digital control interface located on each RF module in the system. SRFC consists of a master bus controller resident on a preprocessor/controller module type, a multi-drop bus, and a slave interface for each RF module on the bus.

The SRFC also has flexible interface driver options for the master-slave bus interface. The typical driver implementation for the master-slave bus is a commercial low voltage differential signal (LVDS) type, but this can alternatively be an RS-485 type differential driver which allows for a much longer length bus (tens of meters instead of a few meters) albeit at a lower data rate.

SRFC concept features have been designed to handle interface requirements for any RF module types that would be resident in a multifunction RF subsystem. Specifically, it satisfies

the goals of a low noise, low cost, small board area, low latency interface that were determined to be requirement drivers for RF module type interfaces.

6.2 PREPROCESSOR ARCHITECTURE AND DATA DISTRIBUTION STUDY

6.2.1 Study Overview and Objective

A trade study was initiated to determine the best preprocessor configuration to support future fighter radar architectures. One of the key drivers for this study was the fact that peak data transfer rates were unlikely to be sustainable in a realizable Fibre Channel network

The first step was to utilize switched Fibre Channel network simulation results to determine the practical limit on sustainable data transfer bandwidth. Initial results looked promising. When routing overhead and message size limitations (imposed to control latency) were taken into account, an average data transfer bandwidth of 80 Mbytes/sec seemed achievable. However, more sophisticated modeling of the unified network processor architecture reveled that for busy-able processing elements, the average data transfer bandwidth dropped to 40 Mbytes/sec for a 1 GHz switched Fibre Channel unified network.

The second step was to compile the average I/Q data transfer requirements of a strawman radar mode suite. Analysis of the data led to the conclusion that while a single Fibre Channel could support two receive channels of streaming data to a non-busyable processing element, that same single Fibre Channel would actually support only one receive channel if we wanted to connect directly to a unified network switch.

This conclusion led to the introduction of a Data Distribution function to the notional radar architecture illustrated in Figure 6.2.1-1. The Data Distribution function is intended to support several system architectural goals:

- Avoid I/Q data loss due to network blockages
- Improve utilization of signal processing nodes
- Reduce/manage data network bandwidth requirements
- Control of data flow configuration independent of RF sensor hardware configuration
- As a key element of the RF electronics/processor software isolation layer, hide RF sensor implementation and complexity from signal processing software developers
- Simplify RF sensor integration and testing support for software debugging

The Data Distribution function's purpose is to route I/Q data to signal processing nodes according to a pattern specified in a message from the Core Processor. The Data Distribution function collects and stores the I/Q samples output from the Video Processor ASICs and outputs those samples on command to the Fibre Channel I/Q data interface. This capability prevents the potential loss of I/Q samples due to Fibre Channel network blockages, and allows the radar system designer to better allocate data network bandwidth by taking advantage of the generally lower average I/Q data rates for those radar modes which have a low receiver duty factor.

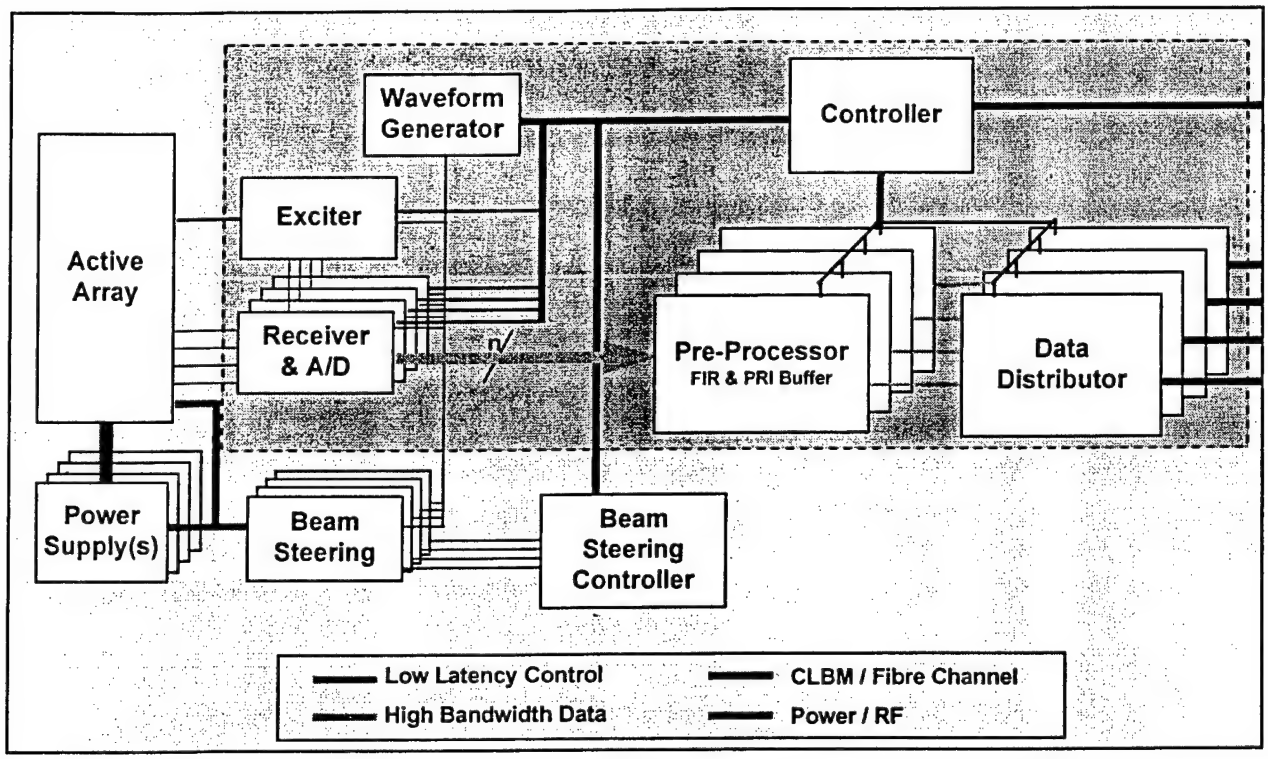

Figure 6.2.1-1. Notional Radar Architecture Featuring A Data Distribution Function

The data buffer function supports the simple, bulk memory like, I/Q data abstraction illustrated in Figure 6.2.1-2 in which the I/Q data from each receiver channel is written independently into consecutive buffer memory locations. The data for each processing node is then read out of the buffer using a string and skip addressing scheme. This abstraction allows much of the RF sensor implementation and timing complexity to be hidden from the signal processing software, and also allows the I/Q data flow to be controlled independently of the RF sensor configuration.

In addition, string and skip addressing provides the opportunity to "corner turn" the I/Q data while sending it on to the processing nodes. Specifically, for each channel I/Q data is written into memory in range sequence, one PRI at a time (row ordered). By selecting the correct string length and skip distance, the data can be read out in PRI sequence (column ordered). This process of sending one or more range bins of all PRIs to a processing node is referred to as "corner turning" and is often useful when doppler filtering is the first signal processing step.

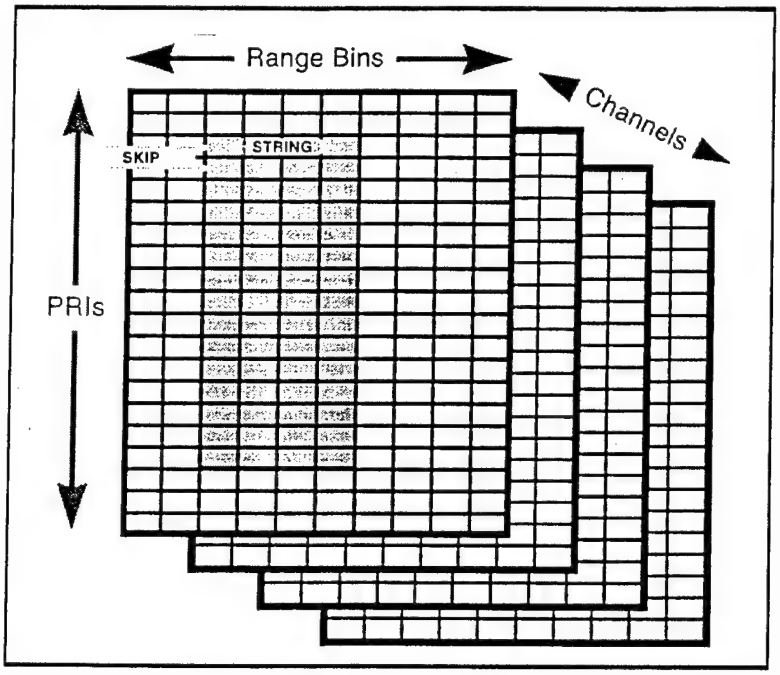

Figure 6.2.1-2. String/Skip Addressing of a Three Dimensional Data Object (e.g., I/Q samples ordered by Range Bin, PRI, and Channel) Supports the Natural Patterns of Access Nneeded By Radar Modes

6.2.2 Options Considered

A trade study was undertaken to determine the optimum system configuration. The four options considered are described in Table 6.2.2-1. For configuration 4 it was assumed that the Data Distributor would possess the full functionality of a Global Bulk Memory similar to that implemented in the F-22 Common Integrated Processor. It was also assumed that the processing nodes would be able to read/write intermediate results from/to the Data Distribution memory in addition to retrieving I/Q data.

TABLE 6.2.2-1. PREPROCESSOR/DATA DISTRIBUTION CONFIGURATIONS SELECTED FOR FURTHER EVALUATION

#	Option	Preprocessor Output Interface Type	Number of Preprocessor Output Ports	Corner-Turn Output Ports into Switch
1	Preprocessor with PRI Buffer, no Corner Turning Data Distribution Hardware	Unified Network Protocol (FC + Labeled Messages)	1-2 Receiver Channel(s) per 1 Fibre Channel	(Not Applicable)
2	Preprocessor with PRI Buffer, separate Corner Turning Data Distributor (could either be in CISP or LCRE, but not part of VP)	Point-to-Point Fibre Channel	2 Receiver Channels per Fibre Channel	1 Receiver Channel per Fibre Channel
3	Preprocessor with PRI Buffer and Corner Turning Data Distribution Hardware	Unified Network Protocol (FC + Labeled Messages)	(Not Applicable)	1 Receiver Channel per Fibre Channel
4	Preprocessor with PRI Buffer, separate Corner Turning Data Distribution Hardware in CISP	Unified Network Protocol (FC + Labeled Messages)	1-2 Receiver Channel(s) per 1 Fibre Channel	1 Receiver Channel per Fibre Channel, plus 2 Fibre Chan.

6.2.3 Evaluation Criteria

The evaluation criteria used in this trade study are shown in Table 6.2.3-1.

TABLE 6.2.3-1. PREPROCESSOR ARCHITECTURE/ DATA DISTRIBUTION TRADE STUDY EVALUATION CRITERIA

Evaluation Criteria
Non-Recurring Engineering Cost
Module Design Cost
Data Distribution Software Development Cost
Recurring Cost
Number of Module Types
Number of Total Receiver Modules
Number of Total Core Processor Modules
Risk
Receiver Hardware Design Risk
Core Processor Hardware Design Risk
Data Distribution Software Design Risk
Mode Software Design Risk
Performance
Processing Reserve
I/Q Bandwidth Reserve
Routing Flexibility
Growth
Spare Core Processor Slots
Spare Receiver Slots
Spare Fibre Channel Switch Ports

6.2.4 Results and Recommendations

Option 3, the single module, two channel preprocessor design combining Preprocessor and Data Distribution functions received the highest trade study score and is the recommended approach.

6.3 RECEIVER FUNCTIONAL PARTITIONING STUDY

6.3.1 Study Overview and Objective

The functional partitioning of the Receiver and Preprocessor modules has evolved over time due to changes in form factor as well as changes in requirements. As of mid 1998, the plan was to develop a two channel Receiver module and a four channel Preprocessor module, both in a SAM form factor. Based on the results of the Data Distribution trade study described in Section 6.2 herein, the baseline approach for the Preprocessor was changed from a four channel module to a two channel module. This allowed incorporation of the Data Distribution function into the Preprocessor module. It also resulted in a more flexible partitioning. Rather than have a two channel Receiver module and a four channel Preprocessor, both modules were now two channel modules, which allows Receiver Subsystems to be efficiently built in two channel increments rather than four channel increments.

The next logical step was to explore the feasibility and desirability of a single channel Receiver module which would incorporate all of the functions currently assigned to both the Receiver and Preprocessor modules. This module would accept an RF input and provide a digitized I/Q output. Key benefits include lower non-recurring, recurring, and support costs because two module types are consolidated into one. Also, channel to channel isolation could be improved, and fault isolation would be simplified with only one module in the receive path. Drawbacks include the potential for increased noise due to the collocation of analog and high speed digital circuits on the same module. Also, functions such as microprocessors and control interfaces which were shared between the two channels on a module would have to be duplicated on each single channel module, requiring more module real estate.

6.3.2 Options Considered

Two options were considered in this trade study. Option one, the baseline option, was the two channel Receiver and Preprocessor partitioning, shown in Figure 6.3.2-1. Option two was the single channel Digital Receiver module which combined the functions of the baseline Receiver and Preprocessor modules. This option is shown in Figure 6.3.2-2.

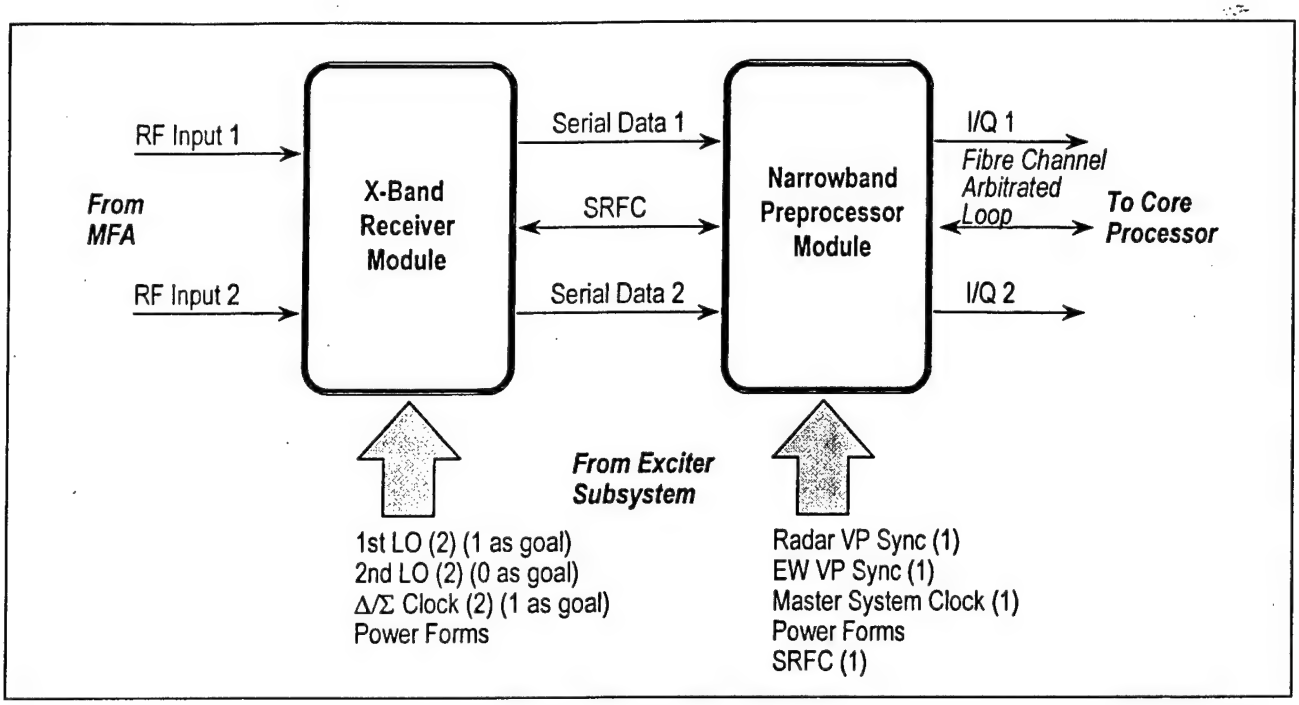

Figure 6.3.2-1. Option 1 – Two Channel Receiver and Preprocessor Modules

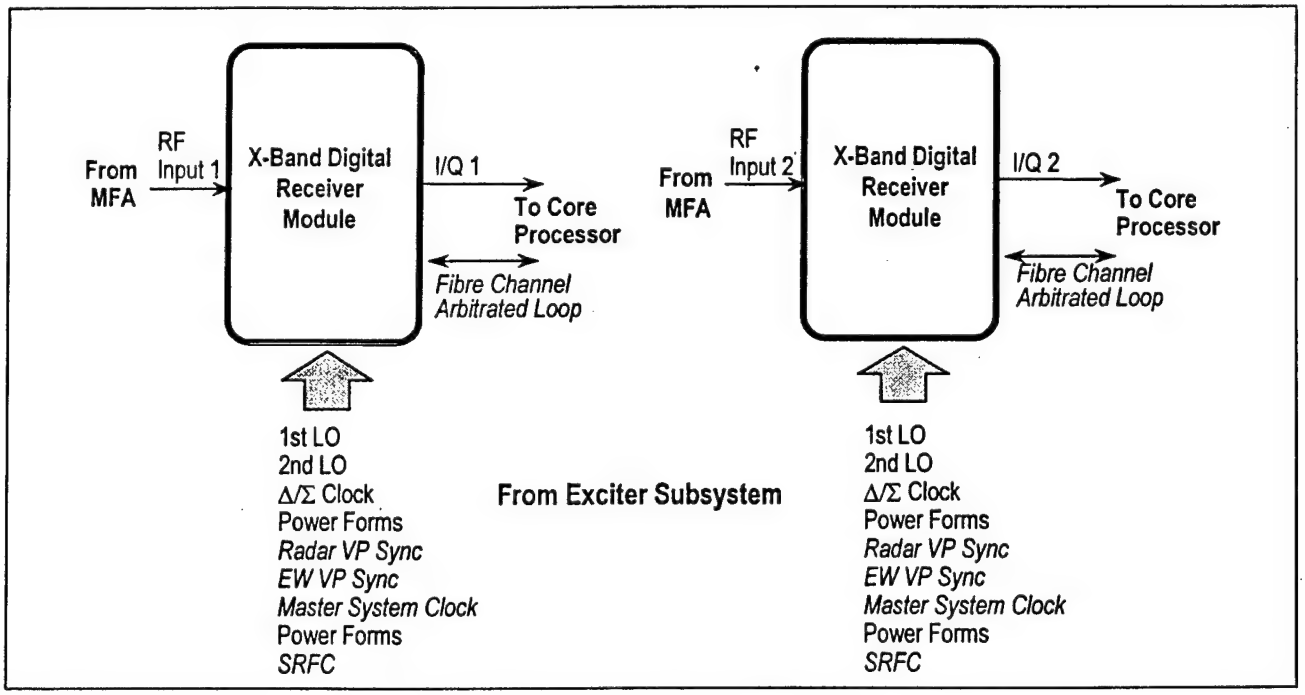

Figure 6.3.2-2. Option 2 – Single Channel Digital Receiver Module

6.3.3 Evaluation Criteria

Once the study objective and options were defined, the next step was to determine the evaluation criteria and specific metrics against which each option would be assessed. Table 6.3.3-1 lists the evaluation criteria for this study.

6.3.4 Results and Recommendations

Because airborne fighter platforms are a primary target for insertion of the MODRFS technology and products, size and weight were key considerations in this study. One of the primary concerns during the evaluation of the single channel receiver approach was the fact that control and microprocessor functions that were shared in a two channel configuration would have to be duplicated on each single channel module, creating more "overhead" hardware. Specifically, this overhead hardware includes a microprocessor subsystem which supervises module operation, Fibre Channel network interface circuitry which receives module control commands from, and provides module status to, the Core Processor, serial RF control bus circuitry which controls the Receiver and Exciter modules, and clock distribution circuitry. It is estimated that shared components occupy approximately 40% of the total Preprocessor module area, with the remaining 60% being used by channel specific components (30% per channel).

Both sides of the Receiver module are identical, with each side containing all of the components necessary to receive an X band input and convert it to high speed digital data. In order to create a single channel, RF to I/Q Receiver module, all of the necessary digital processing, control and interface components would have to fit on one side of a SAM module. Because 40% of the area of a two sided module, which translates to 80% of one side of a module, is required for overhead, only 20% remains for the channel specific components. The end result is that all of the components required for a single channel, RF to I/Q Digital Receiver module far exceed the area available on the module. Therefore, this option is currently not feasible and the recommendation is to proceed with development of the baseline configuration.

It should be noted that, over time, the size of digital components will continue to shrink while their density and processing speed increase. For this reason, longer term (3 to 5 year) roadmaps

TABLE 6.3.3-1. RECEIVER FUNCTIONAL PARTITIONING TRADE STUDY EVALUATION CRITERIA

Evaluation Criteria	*Metric*
Recurring Cost	Percent increase or decrease
Support Cost	Percent increase or decrease
Technical Risk	High, Medium, Low
Channel Isolation	Difference in dB
Noise Performance	Difference in dB
Volume	Difference in number of 0.6 inch pitches for an 8 channel system
Weight	Difference in pounds for an 8 channel system
Reliability	Percent increase or decrease
Maintainability	Impact on fault isolation (good, better)
Growth	Ability to support future growth, including on-board memory and processing (low, medium, high)

should seriously consider the single channel digital receiver approach since it is expected to become feasible with near term technology in that time frame.

6.4 INSTALLATION TRADE STUDIES

Several installation trades were identified in relation to the key "non-functional" requirements identified in Section 2 herein. These trades resulted in varying levels of analysis in order to reach a recommendation. Detailed installation trades are difficult to perform on a program such as MODRFS, which is not targeting a specific platform, because each installation is going to be different from another to some extent. However, by looking at a representative set of potential target applications, it is possible to develop at least a general set of guidelines and recommendations.

6.4.1 Impact of Form Factor and Cooling Method on Commonality

6.4.1.1 Study Overview and Objective. Commonality of hardware and software across multiple platforms and applications is typically acknowledged as a means of reducing development, acquisition and support costs. If a design can be reused, the second user will have a very low non-recurring cost. If two or more users can use the same product, production rates will climb and recurring costs will fall. Once in operation, multiple users of the same product can share a common depot. In addition, if the two or more platforms are collocated (e.g. two aircraft using the same receiver on the same carrier) they may also be able to reduce the total number of spare hardware required.

Form factor and cooling method have a significant impact on the ability to develop modules that can be used on multiple platforms. It is common knowledge that there is no standard form factor or cooling method in place within each service, let alone across all services. In fact, individual platforms typically contain modules in various form factors. The objective of this study was to determine if any useful design guidelines could be developed regarding form factor and cooling.

6.4.1.2 Results and Recommendations. Several platforms were surveyed to determine whether some guidelines could be developed which would be useful in guiding the development of future modular digital receiver building blocks. Table 6.4.1.2-1 shows the results of this initial survey, which assessed the form factor and cooling of receiver hardware similar to that being developed by MODRFS.

As can be seen in Table 6.4-1, most systems containing receiver hardware similar to that being developed by MODRFS use either the SAM or SEM-E form factor. A few systems use other standards such as VME, or they use a unique form factor designed to maximize use of a specific space on a specific platform. In general, there does not seem to be a "best choice" between SAM and SEM-E. Therefore, the form factor of choice will most likely continue to be traded in the future. Ultimate recommendations will be based on the space available on a specific platform, the functions being performed by the modules, and the current state of technology at the time of the trade. However, with the current drive towards standardization wherever possible, and the knowledge that most systems use either SAM or SEM-E, guidelines can be developed such that key receiver building blocks are designed to fit efficiently on either SAM or SEM-E formats.

TABLE 6.4.1.2-1. FORM FACTOR AND COOLING METHOD SURVEY RESULTS

	Form Factor			Cooling Method		
Platform	*SAM*	*SEM-E*	*Other*	*Conduction*	*Liquid Flow Through*	*Air Flow Through*
F-15 Radar	X					X
F/A-18 Radar	X					X
F/A-18 EW			X			X
AV-8B Radar	X					X
F-22 Radar, EW & CNI		X		X		
Comanche		X		X		
JSF Radar	X				X	
JSF EW & CNI		X		X		
Global Hawk			X			X

NOTE: SAM measures approximately 9.3 inches x 5.4 inches
SEM-E measures approximately 6 inches x 6 inches

In general, it is recommended that building block development focus on developing modular components that can be used to efficiently build modules in a variety of form factors. This approach provides the most flexibility for module designers who will always be required to satisfy the needs of a specific platform in the most efficient manner possible. At a minimum, the building blocks should be designed for efficient use on both SAM and SEM-E form factors, since they are the most common form factors currently in use. It is also recommended that modules such as an X Band Receiver module, be developed in a SAM form factor. The reasoning behind this recommendation is that SAM supports the majority of legacy systems and, since there is no clear advantage between SAM and SEM-E for future platforms, SAM can just as easily support future platforms as SEM-E.

6.4.2 Environment

6.4.2.1 Study Overview and Objective. Environment requirements, such as temperature, vibration and electromagnetic compatibility, have been identified as key non-functional requirements that could have a significant impact on the development of modular receiver building blocks. Similar to form factor and cooling method, environment requirements can vary significantly depending on the specific application. However, for component level building blocks it can also be argued that the impact of environment requirements can be minimized by adding layers of isolation at a module level, unit level, and/or platform level. These layers of isolation can include EMI shielding, vibration isolation, and potentially thermal isolation. Module level building blocks can also be isolated from the environment to a certain extent, but the options are more limited compared to component level building blocks.

6.4.2.2 Results and Recommendations. Rather than attempt to document all potential environment requirements for every target application and platform, and then attempt to design building blocks to the worst case environments, a simpler approach is recommended. It is recommended that building block designs attempt to meet the environment requirements typical of a fighter aircraft with short take-off and vertical landing (STOVL) capability, such as the

AV-8B or the STOVL version of a Joint Strike Fighter (JSF) aircraft. This is a very stringent environment, but does not impose the even more stringent requirements required by space based systems. It is recommended that the use of modular receiver building blocks in space-based applications be accomplished by a separate ruggedization effort, so that all other potential users are not required to pay the additional cost associated with space qualified components. Typical recommended environment requirements for airborne applications are summarized in Table 6.4.2.2-1.

TABLE 6.4.2.2-1. TYPICAL ENVIRONMENTAL REQUIREMENTS FOR AIRBORNE COMPONENTS.

*Environment**	*Requirement*	*Applicable to*
Random Vibration	5 g^2/Hz @10-80Hz 10 G^2/Hz@ 80-100Hz 100 G^2/Hz@ 100-200Hz 1 G^2/Hz@200-1000Hz -6db/Oct@1000-2000Hz 2 hours per axis	All components, with no vibration isolation
Random Vibration	5 g^2/Hz @10-80Hz 10 G^2/Hz@ 80-300Hz 0.5 G^2/Hz@ 300-2000Hz 2 hours per axis	Components with vibration isolation applied
Shock, non-operating	100Gs at 3.msec sine pulse	Components < 1 lbs
Shock, non-operating	40Gs at 11 msec sine pulse	Components > 1 lbs
Shock, operating	75 Gs at 5 msec sine pulse	Components < 1 lbs
Shock, operating	20 Gs at 11 msec sine pulse	Components > 1 lbs
Acoustic Noise	130dB SPL@20-100Hz 140dB SPL@100-1000Hz -6dB/oct@1000-1000 50 hours	All components
Acceleration	25 Gs any direction	All components
Storage temperature, non-operating	-63C to 95C	All components
Operating temperature (case)	-40C to 95C	All components
Altitude	-200 to 70000 feet	All components
Explosive atmosphere	Non-ignition of jet fuel @ 95C from –200 to 70000 feet	All components
Humidity**	30C – 60C, 85-95 % relative humidity, 96 hours, and condensation	All components
Salt fog**	5% salt, 1%SO(2), 10ppm NO(2), 220 micrograms/m^3 ozone, 500 hours	All components
Fungus**	Tropical climate fungus exposure	All components
Sand and Dust**	Sand and dust exposure	All components
Fluid resistance**	Resistance to solvents, jet fuel, coolant, and hydraulic fluids	All components

*Unless otherwise specified all conditions are operating

** Moisture/corrosion and environmental barriers may be applied to protect against this requirement

6.4.3 Backfit Into Legacy Systems

6.4.3.1 Study Overview and Objective. The ability to backfit future receivers into legacy systems is an important consideration in the definition and development of the building blocks. One key reason for its importance is the fact that there are more upgrade programs than there are brand new programs. Therefore, if future receiver development is focused only on new systems, a significant portion of the potential target platforms will be excluded.

Insertion of new equipment into existing aircraft normally occurs for one of two reasons; 1) to provide improved functionality or performance, and/or 2) to replace equipment whose parts are no longer available due to parts obsolescence. When new functionality is provided, interfaces to other avionics equipment will invariably change even if only to update the control interface to command the new functionality. This has a tendency to drive costs due to the typical partitioning of legacy systems and the close coupling of hardware and software. When new functionality is not provided, the cost impact can still be significant if the needs of the legacy aircraft (i.e. Group A modifications) are not taken into account early in the new system's design process. Specific actions that can be taken to minimize Group A impacts include minimizing interfaces within systems and subsystems, providing adequate modularity within system designs, and designing system and aircraft interfaces to be flexible for growth or replacement as technology changes.

A study to evaluate the feasibility of insertion of a MODRFS narrowband receiver into legacy aircraft was conducted. The trade study assessment centered on the cost effectiveness of taking the MODRFS narrowband receiver and inserting it into the legacy aircraft with varying levels of modification to other hardware and software. Performance impacts to aircraft operational capabilities were also considered for each alternate insertion configuration.

6.4.3.2 Backfit Options Considered. Four options which would support backfit of a new technology receiver subsystem into a legacy radar system were identified, and are described in Table 6.4.3.2-1.

6.4.3.3 Backfit Trade Study Results. The first option considered was replacement of only the receiver subsystem. This option is attractive because it has the lowest impact on the platform and provides the lowest acquisition cost. System performance improvement would be minimal if inserted in a system with a conventional Mechanically Scanned Array and a legacy processor, but it could be considered if a receiver replacement is required due to parts obsolescence or poor reliability. However, there are significant drawbacks to this option which likely make it not feasible for most applications. These drawbacks include the fact that the receiver subsystem is highly dependent on specific clocks, local oscillators, and control signals from the exciter subsystem. It is unlikely that a legacy exciter would be able to provide these critical signals. Also, insertion of the receiver subsystem would require some sort of interface module to allow the subsystem to communicate with the legacy processor. Additionally, there would be a significant impact to the mode software required to utilize and control this new receiver subsystem. Finally, insertion of the receiver subsystem into a legacy system which utilizes a Mechanically Scanned Array would require the addition of a low noise amplifier module in front of the receiver in order to maintain a reasonably low noise figure. This could also be accomplished by removing the preselect filter function and replacing it with a low noise amplifier. Because of these drawbacks, it is unlikely that insertion of a new receiver subsystem would be feasible in most applications without other significant changes.

TABLE 6.4.3.2-1. OPTIONS FOR BACKFITTING A NEW TECHNOLOGY RECEIVER SUBSYSTEM INTO A LEGACY RADAR SYSTEM

Option	*Description*	*Benefits*	*Drawbacks*
1	Replace Receiver Subsystem	• Lowest impact on platform • Lowest acquisition cost • Improved Receiver reliability	• Probably not feasible due to dependence on specific clocks, control and LOs from Exciter, which are not likely to be available in legacy exciter • Significant software impact • Requires special interface hardware • Low noise amplifier module would be required to support a Mechanically Scanned Array (MSA) • Minimal system performance improvement • Does not address likely Core Processor obsolescence issue
2	Replace Receiver/Exciter Subsystem	• Low impact on platform • Low acquisition cost • Improved Receiver/Exciter reliability	• Significant software impact • Requires special interface hardware • Low noise amplifier module would be required to support a MSA • Minimal system performance improvement • Does not address likely Core Processor obsolescence issue
3	Replace Receiver/ Exciter Subsystem And Core Processor	• Increased system performance • Increased system reliability • Lower parts obsolescence risk • Ability to leverage SHEL concept and existing system software libraries	• Low noise amplifier module would be required to support a MSA • Potentially significant impact on platform interfaces • Limited system performance with MSA
4	Replace Entire Radar System	• Highest performance • Highest reliability/supportability • Lower parts obsolescence risk • Ability to leverage SHEL concept and existing system software libraries	• Highest acquisition cost • Highest impact on platform

The second option considered was replacement of the receiver and exciter subsystems. This option eliminated the issue of providing specific clocks, LOs, and control, and had the same benefits as replacement of only the receiver subsystem, but at a higher acquisition cost. However, in addition to higher acquisition cost, this option also has many of the same drawbacks as the previous option. There is still a significant system software impact, a need for an interface module between the receiver and core processor, and a need for an LNA in front of the receiver. Also, insertion into a legacy system which utilizes an MSA and legacy processor will significantly limit any improvement to system performance.

The third option considered was replacement of the receiver and exciter subsystems, along with replacement of the core processor. While this option requires an increase in acquisition cost as compared to the previous options, it also provides many benefits and eliminates many

drawbacks. Replacing the processor allows for increased system performance due to increased memory and throughput. It also lowers the software impact because it allows leverage of existing software libraries which have been developed for use with a MODRFS type receiver and exciter. In addition, this options allows implementation of the SHEL concept described in Section 4, herein, which will help mitigate the impact of future hardware and software upgrades. Although a LNA will still be required for insertion into a system using an MSA, replacing the core processor eliminates the need for a special interface module between the receiver and processor. A drawback for this option is the potentially significant impact that changing the core processor may have on the platform interfaces. This is highly platform dependent and must be evaluated on a case by case basis. However, it should be noted that since processors tend to become obsolete more rapidly than other system components, there is a good chance that a legacy system that is a candidate for receiver subsystem replacement is also a candidate for processor replacement. This is particularly true for systems that use non-COTS based components and interfaces.

The fourth option considered was replacement of the entire radar system. Obviously, this option provides the greatest improvement in reliability and system performance, but it also carries the highest development and acquisition costs, and has the highest impact on the platform.

An assessment of these four options resulted in the determination that replacement of the receiver subsystem, with or without replacement of the exciter subsystem, is not likely to be feasible for most applications. The probable impacts on system software and interfaces are simply too great. While replacement of the entire system is certainly a feasible option in some cases, it is not the objective of the MODRFS program to require entire system replacement in order to utilize the MODRFS receiver. Therefore, option 3, replacement of the receiver and exciter subsystems along with replacement of the processor, is the recommended approach. This approach provides the best balance between acquisition cost, platform impact, supportability and system performance. However, in cases where significant increases in system performance and/or supportability are required, replacement of the entire system must be considered.

6.4.4 Power Conversion Study

6.4.4.1 Study Overview and Objective. A significant area of concern in new product development efforts is one of parts obsolescence and new technology insertion. One effect of these realities is that the power supply architecture must be updated to support new parts and technologies when they are inserted into the system. This concern led to a study targeted at minimizing power subsystem impacts when new technology is inserted due either to capability growth or parts obsolescence.

6.4.4.2 Options Considered. Centralized power conversion of primary power to secondary power has been a hallmark of legacy systems. It enables cost and volume efficient designs suitable for airborne applications. More recently, the idea of distributed power conversion has gained acceptance as an effective way to minimize power subsystem disruption due to product updates. This is actually a feature of a solution to the more acute problem of distributing low-voltage high-current power forms. Distribution of high-current power forms has always benefited by local conversion and regulation. This minimizes I-R drops throughout the distribution system and provides improved load regulation. For these reasons, centralized and distributed conversion systems were natural candidates for a power supply architecture study.

An example centralized conversion system would start with an input power conditioner for EMI filtering, in-rush current control, power switching, rectification (if applicable) and bulk energy storage. The next stage would be a multi-tap DC-DC power converter with the highest current power form being regulated. This would convert the primary (rectified) input power to the needed secondary power forms, both regulated and unregulated. It would also provide energy storage for the secondary power. These secondary power forms would then be linearly regulated and distributed to the using modules. Figure 6.4.4.2-1 illustrates an example centralized conversion system.

An example distributed conversion system would still need the input power conditioner and may also require an intermediate (+48v for example) DC-DC converter. The merits of providing intermediate power directly at the unit inputs have been debated elsewhere. For our purposes, it was sufficient to assume that an intermediate converter might be required. This intermediate power would be distributed to the using modules for conversion and regulation locally on the module. An example distributed system is illustrated in Figure 6.4.4.2-2.

6.4.4.3 Evaluation Criteria. Evaluation criteria were developed based on areas of concern with the two candidate architectures. Table 6.4.4.3-1 lists the evaluation criteria and their system impact.

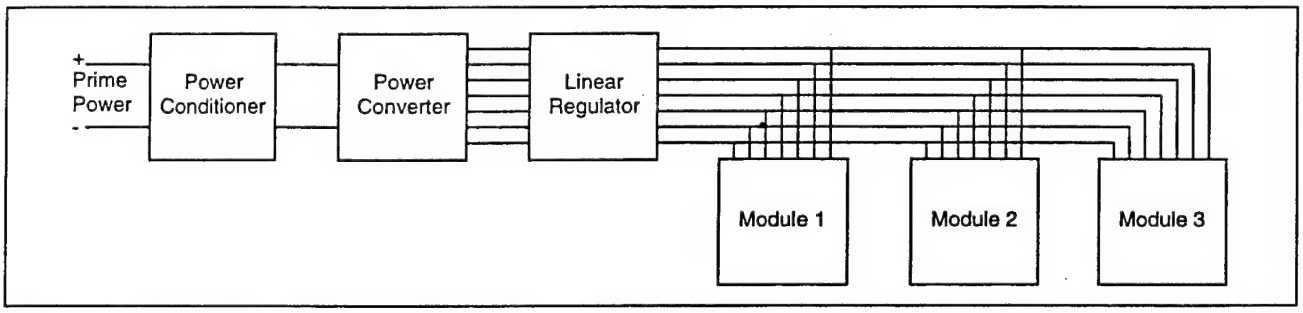

Figure 6.4.4.2-1. Centralized Power Conversion

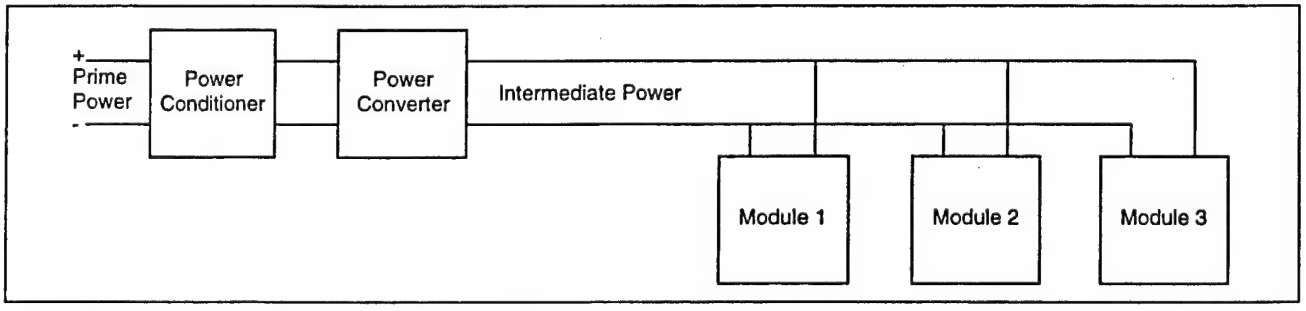

Figure 6.4.4.2-2. Distributed Power Conversion

6.4.4.4 Results and Recommendations

Weight and Volume Impact: For an initial cut, it would seem that a distributed power conversion scheme would save on overall system volume (and therefore, weight and cost). The elimination of a central power converter module and associated linear regulator should result in a more compact system. Generally, however, the multi-output power converter has to be replaced with either an intermediate converter or some other form of regulation. This ensures that the intermediate power form does not force unrealistic requirements for the local converters.

For digital modules this scheme can work. Analog modules typically require twice the number of power forms, tighter regulation and several orders of magnitude better ripple than digital modules. Table 6.4.4.4-1 provides a comparison of typical module power requirements. These performance parameters are difficult to achieve with smaller local converters and regulators. In fact, so much board space would be devoted to power conversion and regulation that the effective packaging density of analog circuits would be severely reduced. This would lead to an increase in the overall number of analog modules in the system. For a representative four channel Modular Digital RF System, the elimination of one power supply module was offset by an increase of 4 receiver and exciter modules. This volume increase is compounded with the addition of more receiver channels. Obviously, this is headed in the wrong direction. In fact, for a modular (parallel) system, the more infrastructure that can be removed from a typical module, the better the volume story becomes. Weight is intimately tied to volume, so it is rational to expect the target system to become heavier with local conversion and regulation.

TABLE 6.4.4.3-1. POWER CONVERSION TRADE STUDY EVALUATION CRITERIA

Evaluation Criteria	*Concern*
Weight and Volume Impact	Weight and volume are always design drivers for airborne applications.
Recurring Cost	All production oriented designs need to minimize recurring costs.
Growth/Technology Insertion Impact	Can drive long-term affordability of system.
Technical Performance Risk (EMI)	Performance requirements elevate importance of EMI suppression.
Non-recurring Cost	An otherwise optimum solution cannot be used if it requires too much investment to develop.

TABLE 6.4.4.4-1. TYPICAL POWER REQUIREMENT COMPARISON

Parameter	*Analog Module (excluding power amps)*	*Digital module*
Number of Power Forms	4–6	2–4
Typical Voltages (VDC)	5–28	2–5
Required Regulation	<2%	<7%
Maximum Current	<5a	<20a
Ripple Magnitude	μVolt	mVolt

Recurring Cost: In airborne electronics applications, volume (and weight) also can gauge cost. As the module count (volume & weight) increases, more infrastructure (connectors, PWBs, converters, heat sinks, etc) is purchased. In addition, any volume and weight increase will require increased prime power, cooling, aerodynamic lift and thrust. All of which contributes to increasing the recurring cost of the aircraft.

Growth/Technology Insertion Impact: The obvious advantage that distributed power conversion offers is one of ease of technology insertions. To achieve higher density and speeds, digital logic designs must move to smaller feature sizes. The finer lines have significantly less dielectric thickness which leads to lower withstanding voltages. In addition, reducing the operating voltage also limits the effects of parasitic capacitances which increases logic speeds. As a result, digital logic is on a progression from 5v to 3.3v to 2.5v to 1.8v, eventually reaching as low as 0.5v. As established components become obsolete, they are often replaced with either equivalent or improved functions in the new logic families. The net result is that a circuit design update to address parts obsolescence must often incorporate new logic power forms. Any new capabilities inserted due to technology advancements will also require newer low voltage power forms. With a distributed power conversion architecture, differing voltage requirements would be provided for by on-module conversion and regulation.

Another advantage to distributed power conversion is preserving module Input/Output capacity while minimizing I-R voltage drops in the distribution network. Assuming that typical modules might dissipate 50w of power, the current required to operate 5v circuitry will be about 10a, whereas 20a will be required to operate 2.5v circuitry. Doubling the required input current doubles the number of I/O pins required to supply module power. By converting and regulating on-module, a higher voltage/lower current supply can be used. This preserves I/O capacity, prevents power I/O changes associated with technology changes and localizes the effects of large step current changes that are common with digital circuits. Power losses due to distribution system I-R drops will also be reduced.

Analog circuits have not driven the same sort of power supply voltage trends that digital circuits have. Some voltage requirements have changed, but in general, the power forms required by analog circuits have not changed significantly over the past 20 years. The trend to lower voltage power forms is just not as decisive as for digital circuits.

Technical Performance Risk (EMI): Two critical performance parameters for radar receivers and exciters are directly influenced by power supply design. They are spurious response and additive noise, cumulatively referred to as spectral purity. Microvolt power supply ripple requirements are often used to achieve the needed spectral purity performance of radar equipment. The required performance for a Modular Digital RF System is demanding enough that radiated emissions as well as common mode noise join the typical ripple specification levied on power supplies. The switching noise associated with the use of on-board converters could make it extremely difficult and risky to achieve the required spectral purity performance. The use of centralized conversion and linear regulation provides many more opportunities to protect from unwanted coupling of power supply noise to the sensitive analog circuits used in a high performance receiver/exciter. Note that this is not an issue with most digital circuits.

Non-recurring Cost: Designing digital modules that contain on-board conversion and regulation is well within the capability of most electronics companies. Designing high

performance radar analog circuitry with on-board conversion and regulation has not yet been attempted. This is due in large part to the cost/benefit ratio of making such an attempt. Many design iterations of local conversion would be required before the feasibility of success could even be quantified. It is very likely that there is no 'recipe' for this type of design, meaning that the problem will have to be solved for each new module configuration. This is a high up-front price to pay for potential benefits that are far from guaranteed.

Recommendation: The results of this trade study are summarized in Table 6.4.4.4-2. The discussions above indicate that each type of circuitry contained in a Modular Digital RF System would best be served by a different power supply architecture. Although digital circuits will work well with either a centralized or distributed power conversion scheme, high performance analog circuits will only work well with a centralized power conversion architecture. For a mixed signal environment such as this, the optimum solution is a mixed power distribution scheme. Retain the central conversion and regulation for analog modules, but provide an intermediate voltage such as +48, +24 or +5 that can be used by digital modules to develop the required final voltages. This preserves power form flexibility where it is most required (digital) and provides a cost and volume effective solution for the analog circuits.

TABLE 6.4.4.4-2. POWER CONVERSION ARCHITECTURE TRADE SUMMARY

Metric	*Centralized Power Conversion*	*Distributed Power Conversion*
Backplane Voltages	±15, ±9, +3.3, +5, +24	+48
Example Module Count	3 Exciter, 4 Receiver, 3 PS	5 Exciter, 6 Receiver, 2 PS
Overall Volume Impact	Baseline	+3 Modules
Recurring Cost	Baseline	+3 Modules, +Infrastructure
Growth Power	Limited to existing power forms	Limited only by supply current
EMI Mitigation	Traditional	Heroic
Non-Recurring Cost	Baseline	+Design iterations

7. ACRONYM LIST

A/A	Air-to-Air
ABRA	Agile Beam Resource Allocator
ADC	Analog to Digital Converter
AFT	Air Flow Through
A/G	Air-to-Ground
AGC	Automatic Gain Control
AMPL	Approved Materials and Processes List
API	Application Program Interface
ASIC	Application Specific Integrated Circuit
AWG	American Wire Gauge
BPF	Band Pass Filter
BW	Bandwidth
CDR	Clock and Data Recovery
CISP	Common Integrated Sensor Processor
CIU	Common Interface Unit
COTS	Commercial Off The Shelf
CNI	Communication, Navigation, Identification
CLBM	Content Label Based Messaging
CW	Continuous Wave
DC	Direct Current
DD	Data Distribution
EC	Embedded Controller
ECM	Electronic Countermeasures
EEE	Electromagnetic Environmental Effects
EIB	Extended Input Band
EMI	Electromagnetic Interference
ENR	Equivalent Noise Reflectivity
ESD	Electrostatic Discharge
ESM	Electronic Support Measure
EW	Electronic Warfare
FC	Fibre Channel
FC	Filter Cycle
FFT	Fast Fourier Transform
FM	Frequency Modulation
FPI	Filter Program Interval
FS	Full Scale
HDL	Hardware Description Language
HPRF	High Pulse Repetition Frequency
IC	Integrated Circuit
I/O	Input/Output
I/Q	In-phase/Quadrature
IAR	Integrated Avionics Rack

IC	Integrated Circuit
ICD	Interface Control Document
IER	Integrated Electronics Rack
IF	Intermediate Frequency
IFF	Identification Friend or Foe
IM	Intermodulation
IP	Intellectual Property
IQE	Image Quality Equation
IREW	Integrated Radar/EW
ISAR	Inverse Synthetic Aperture Radar
ISS	Integrated Sensor System
JSF	Joint Strike Fighter
JTIDS	Joint Tactical Information Distribution System
KB	Kilo Byte
LCES	Low Cost Exciter Subsystem
LCRE	Low Cost Receiver Exciter
LCRS	Low Cost Receiver Subsystem
LFM	Linear Frequency Modulation
LFT	Liquid Flow Through
LNA	Low Noise Amplifier
LO	Local Oscillator
LRM	Line Replaceable Module
LVDS	Low Voltage Differential Signal
M	Symbol for Decimation Ratio
MB	Mega Byte
MFA	Multi-Function Array
MIC	Microwave Integrated Circuit
MNR	Multiplicative Noise Ratio
MODRFS	Modular Digital RF System
MSC	Master System Clock
NF	Noise Figure
NIC	Network Interface Controller
OSA	Open System Architecture
PAO	Polyalphaphaolefin
PHM	Prognostics and Health Management
PIB	Primary Input Band
PM	Phase Modulation
PRF	Pulse Repetition Frequency
PVF	Programmable Video Filter
PWB	Printed Wiring Board
QFD	Quality Function Deployment
REC	Receiver Exciter Controller
RF	Radio Frequency
RFI	Radio Frequency Interference
RNIIRS	Radar National Image Interpretability Rating Scale

RP	Radar Processor
SAM	Standard Avionics Module
SAR	Synthetic Aperture Radar
SEM-E	Standard Electronics Module Type E
SH	Sensor Hardware
SHEL	Sensor Hardware Encapsulation Layer
SNR	Signal to Noise Ratio
SRFC	Serial RF Control
SSB	Single Side Band
STC	Sensitivity Time Control
STOVL	Short Take Off Vertical Landing
T&C	Timing and Control
TBD	To Be Determined
TOE	Time of Effectivity
VP	Video Processor
WPI	Waveform Program Interval